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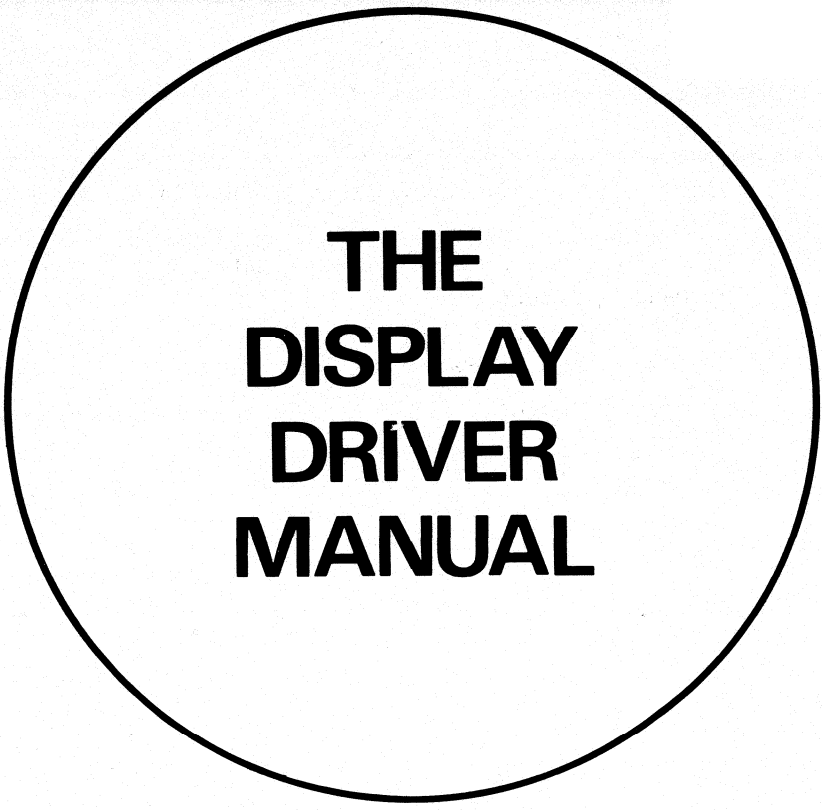

THE DISPLAY DRIVER MANUAL

September 1982

TEXAS INSTRUMENTS

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THE DISPLAY DRIVER MANUAL

VACUUM FLUORESCENT DISPLAYS

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1. INTRODUCTION

Vacuum fluorescent displays, VF, are among the displays that are more commonly used. The versatility in their construction, colour and formats allow the displays to have a wide range of applications.

1.1 Display Construction

The VF display has a construction very similar to a triode valve. It consists of a number of grids and anodes plus a single cathode-heater, encapsulated in an evacuated glass envelope.

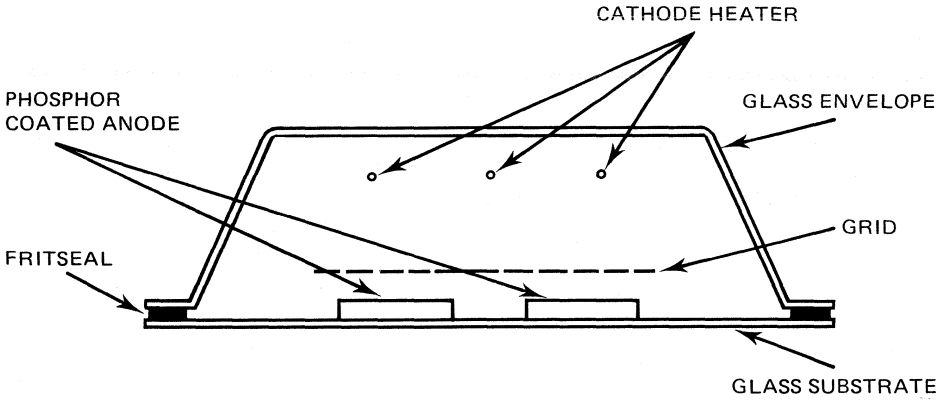


Figure 1.1 Cross-section of a Vacuum Fluorescent Display

Thermionic electrons are emitted from the cathode and accelerated by the anode and grid. After passing through the grid the electrons hit the phosphor coat on the anode. The energy gained by the electrons is enough to allow the phosphor to fluoresce.

Different designs of anode areas mean that dot matrix, segmented, bar graphs and custom displays can be made available. The use of a variety of different phosphors enables the use of multiple colour displays.

1.2 Anode and Grid Biasing

Typical operating ranges of a V.F. display are shown in Table 1.1.

TABLE 1.1 VFD Operating Ranges

PARAMETER	MIN	MAX
Cathode Voltage	0.4V a.c.	10V a.c.
Grid/anode Voltages	24V p-p	70V p-p
Cathode Current	20mA a.c.	250mA a.c.
Grid Current	2.5mA p-p	30mA p-p
Anode Current	2.5mA p-p	30mA p-p
Power Dissipation	14mW/char.	125mW/char.

Ideally the grid potential (Ec) should be biased at 50% of the anode potential (Eb), though practically they can be at the same potential to minimise power supply and driver logic complexity.

The capacitance of the grid due to space charge effects increases when the anode and grid are at the same potential, but this isn't found to be a problem as the capacitance is small.

The anodes and grids operate in a logical AND operation, hence both have to be "on" to select a display element or pixel. Normally either the grids or anodes are commoned in order to reduce external wiring thus giving rise to displays that are either static or dynamic respectively.

Different phosphor coats on the anode segments can be used to create different colours, though the efficiences of the phosphors vary, resulting in different intensities.

1.3 Cathode Biasing

A d.c. bias voltage (Ek) is applied to the cathode to ensure that when the grids and anodes are switched off a negative potential occurs between them.

This reduces switch off time by repelling any thermionic electrons emitted by the cathode.

In addition to the bias voltage applied to the cathode a heating voltage (Ef) is sometimes applied to create the thermionic electrons needed for conduction. The heater voltage should be a.c. If a d.c. voltage is used a potential drop will occur across the cathode, creating variations in cathode-anode and cathode-grid potentials at either end of the display. This results in a variation of intensity across the display.

Eb, Ec – Anode, Grid potentials
Ef – filament heating voltage
Ek – filament bias voltage

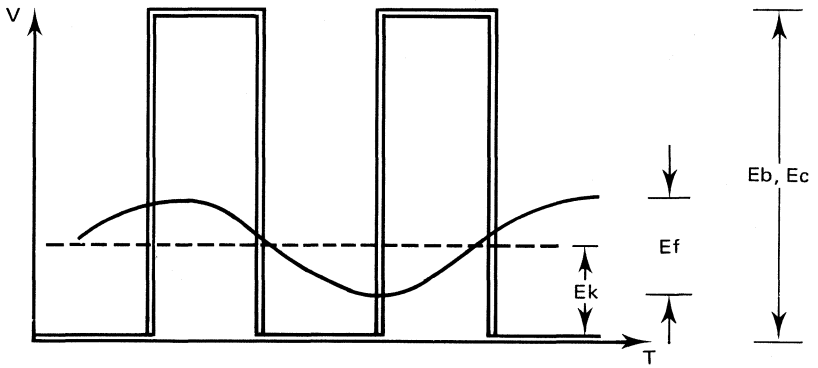


Figure 1.2 Biasing potentials for a V.F. Display

1.4 Switching Characteristics

The anodes and cathodes appear as capacitive loads (Typ 2-5pF) with an associated parallel resistance (Typ 50kΩ) giving rise to the typical switching characteristics shown in Figure 1.3.

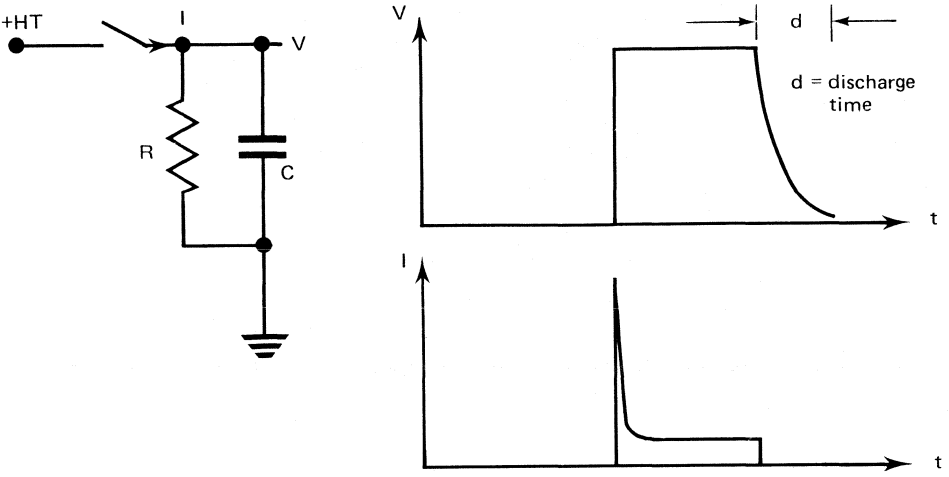


Figure 1.3 Switching characteristics of V.F. Grids and Anodes

When switch off occurs residual capacitance charge takes time to discharge through the resistance R. The switch off time of the V.F. display must be comprehended when multiplexing display data, otherwise segment ghosting can occur. The ghosting can be minimised by using

a) Active turnoff, to minimise discharge time.

b) A blanking period ensuring complete discharge of the anodes and grids before a new character is displayed, commonly called the interdigit blanking time.

2. V. F. DISPLAY TYPES

Vacuum fluorescent displays generally come in two basic forms, which dictate the driving technique that should be used.

2.1 Static Displays

Static displays are non multiplexed, hence for a given display state, the data applied to the display is constant. This is achieved by connecting all the grids to the supply voltage and controlling each segment independently. Consequently static displays tend to have a small segment count as the pin count for larger displays is not practical or economical.

Although static displays may not be practical for large displays, in comparison to dynamic displays the data processing overheads are much smaller, since it needs no refresh.

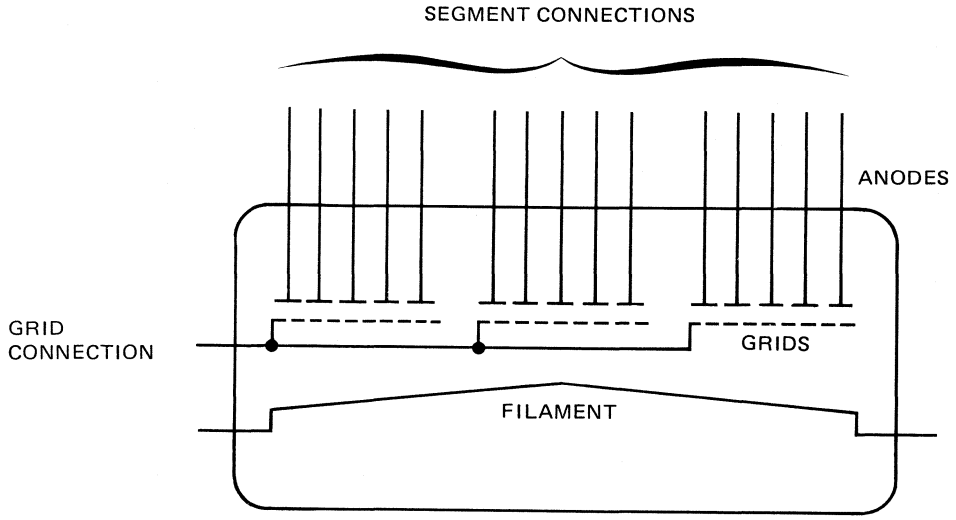


Figure 2.1 Internal Connection of a Static Display

2.2 Dynamic Display

Dynamic displays differ from static displays in that each character is multiplexed. Character information is entered on a set of anode lines, where each line controls corresponding segments in each character. The character location is defined by a set of independently controlled grids which provide a logical AND operation with the anode lines.

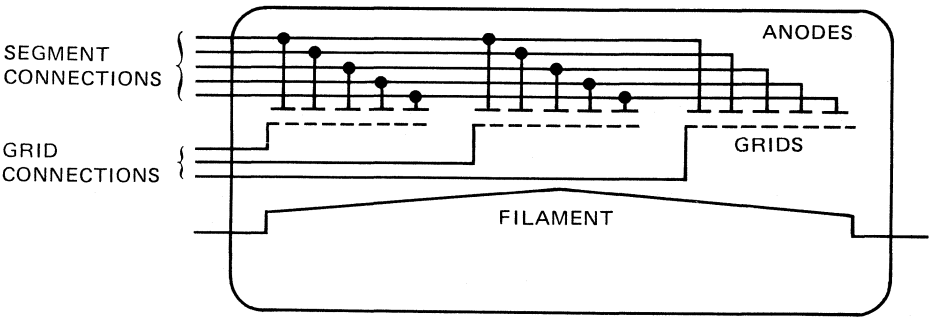


Figure 2.2 Internal Connections of a Dynamic Display

Each character has to be individually selected and displayed to complete the display frame. For continuous operation the frame must be refreshed at a minimum of 60Hz. Higher refresh rates might be required as vibrations can cause stroboscopic effects.

Dynamic displays have significant advantages over static displays such as

- Low pin count
- Reduced driver count

Conversely continuous refreshing and character multiplexing increases the data processing overheads.

3. V.F. DISPLAY DRIVES

A general systems approach to the problem is shown in Figure 3.1. The data processing unit formats the data for the display and transmits it along a set of serial data lines. The serial data is converted to a parallel format and interfaced from TTL/CMOS logic levels to high voltage levels for V.F. display control.

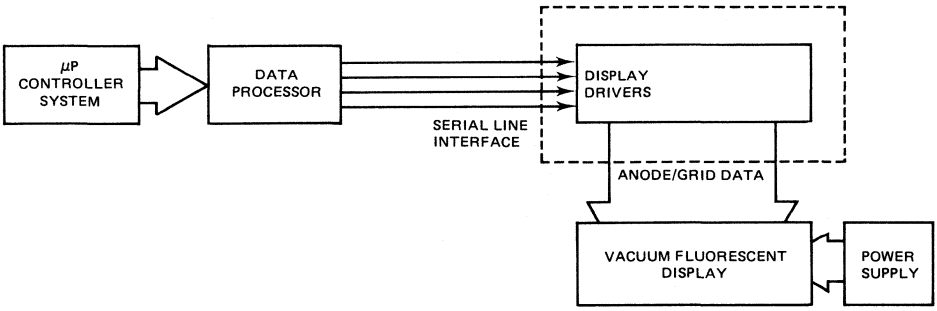


Figure 3.1 Typical Display Control System

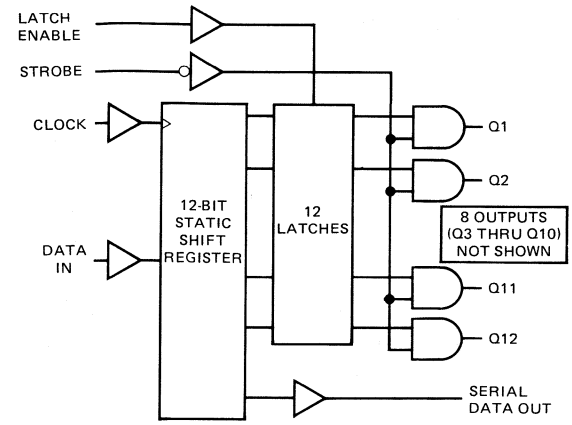
Optimisation of the display driver section will result in a number of advantages:—

- Lower component costs
- Minimisation of board area
- Space saving
- Lower production costs
- Minimisation of wiring
- Remote display driving

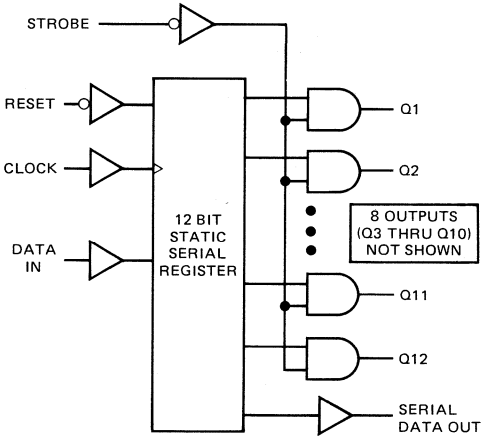
3.1 Display Drivers

The SN75512A, SN75513A and SN75518 are a set of vacuum fluorescent display drivers designed to encompass many of the systems requirements outlined in the previous section.

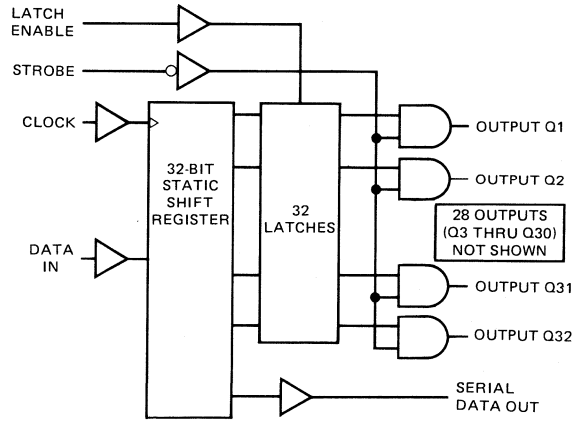
Use of the monolithic BIDFET technology has allowed a mix of large scale integration, LSI, and high voltage devices on the same integrated circuit, making the systems design simpler.



SN75512A



SN75513A



SN75518

Figure 3.2 Display Driver Schematics

It can be seen from the schematics that the devices come in latched and non-latched output versions. The latched output devices allow the data to be loaded while the display is active. This facility reduces the data rate required to load the display in comparison to non-latched output devices, whose data is loaded in the inter digit blanking time.

Non-latched devices are ideal for strobing applications on multiplexed displays.

3.2 Driving Static Displays

Taking into consideration the construction of static displays, described earlier, the control of these displays becomes relatively simple. Any of the display drivers, mentioned earlier, may be used. Data is entered into the devices which are cascaded until the bit length of the shift register is long enough to contain the number of segments required.

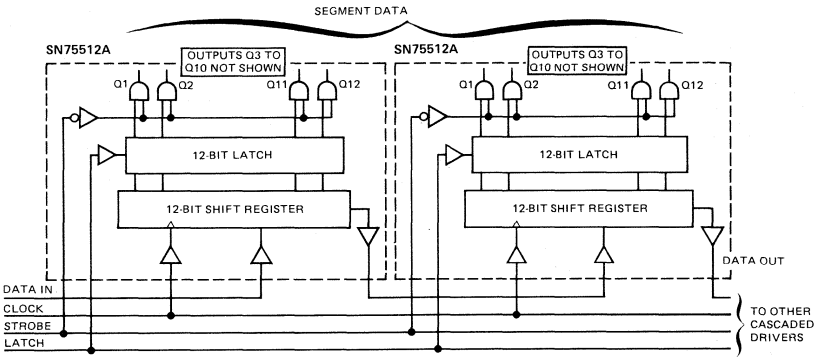


Figure 3.3 Cascaded Static Display Driving

3.3 Driving Dynamic Displays

The need to multiplex data for a dynamic display leads to a large variety of drive techniques. These can be covered with three main design philosophies.

3.3.1 Cascaded Driving

A technique ideal for small dynamic displays involving a number of cascaded drivers. The data is entered on one serial bit stream and the final parallel output contains segment and grid information.

The display driver configuration is the same as shown in Figure 3.3 except that the serial bit stream contains grid information as well as segment information. Figure 3.4 shows a typical string of information that could be used in a 10 segment 14 character display.

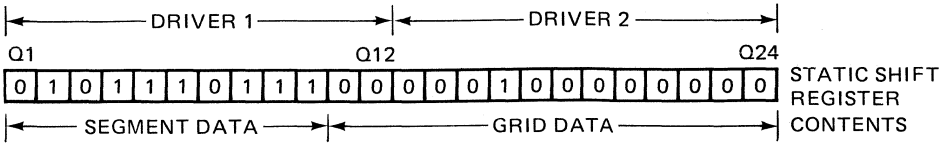


Figure 3.4 Single Bit Stream Dynamic Display Drive Data

3.3.2 X-Y Driving

The grid and anode information is split into two serial bit streams so that the display is addressed in a matrix format. The number of control lines doesn't necessarily increase in proportion to the number of individually controlled devices as the strobe, clock and latch lines can be common.

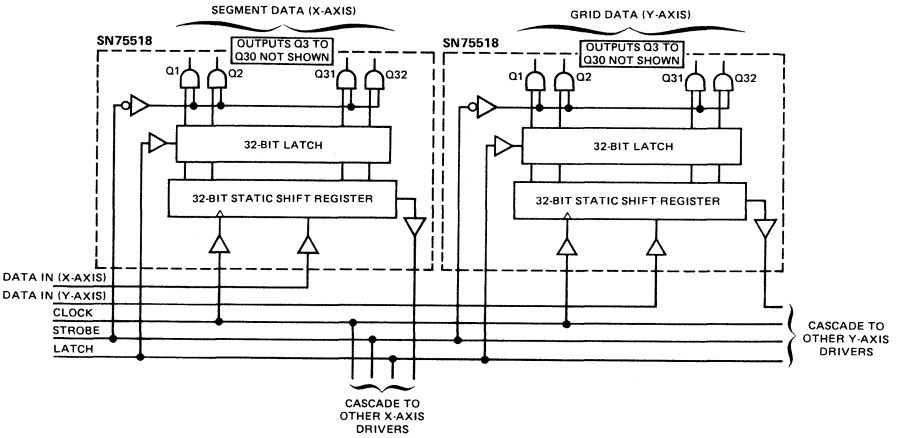


Figure 3.5 X-Y Driving Technique

3.3.3 Multiple Colour Segment Driving

Displays which have combinations of different phosphors to produce different colours, don't necessarily need a number of anode potentials to normalise the intensity. When a common anode potential is used variations in the mark-space ratio of segment strobing can be used instead.

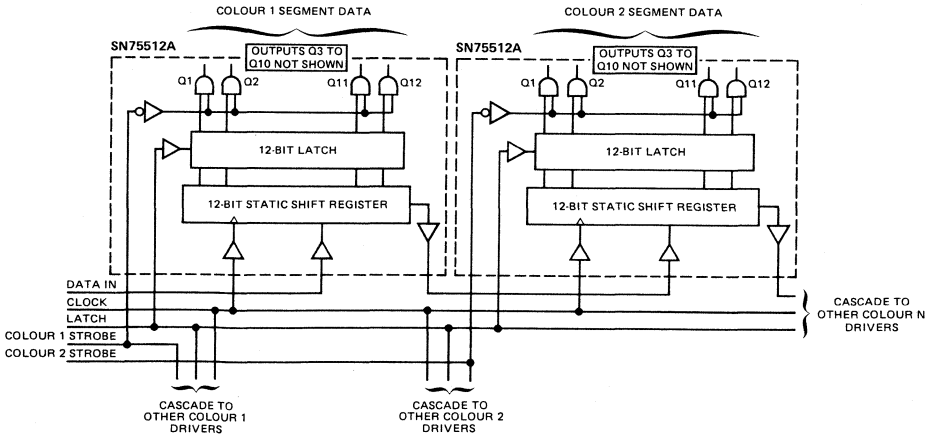


Figure 3.6 Multiple-Colour Segment Driving

Advantages and Disadvantages of V.F. Display Driving

Display drivers:—

- Interface to most V.F. Displays
- Cascade to Service Large Area Displays
- Interface Directly to TTL and CMOS
- Reduce I/O Overheads

Advantages/Disadvantages of Displays with Drivers

Static vs Dynamic

Static	Dynamic
Advantages	Advantages
• Latched Display (Display Memory)	• Low Package Count/Segment
• Low Control Overhead	• Low Display Pin Count/Segment
	• Best Power Efficiency/Segment
Disadvantages	Disadvantages
• Reduced Power Efficiency	• High Control Overhead
• High Display Pin Count/Segment	• High Input Data Rates
• High Driver Package Count/Segment	

Figure 3.1 Summary Table

Driving Vacuum Fluorescent Displays

John D. Spencer
Linear Circuits Division

INTRODUCTION

The Vacuum Fluorescent Display (VFD) operates on the principle of a triode vacuum tube. In the VFD, however, the anode is coated with phosphor which emits light when electrons from the cathode strike it at sufficient energy. The blue-green color given off is bright clear and pleasing to the eye. The VFD is available in dot matrix, segmented and dot character arrangements in a wide variety of sizes. The flat panel construction low operating voltages and power consumption make VFD an attractive option in many display applications.

THE VFD PANEL

Construction

The VFD is composed of three basic elements, the grid, anode and cathode, contained in a glass envelope which provides the vacuum environment required for proper VFD operation (Figure 1).

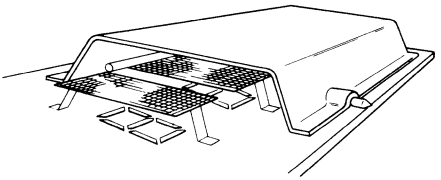


Figure 1. Vacuum Fluorescent Display Construction

The cathode is an oxide-coated tungsten filament which, when heated by a current, emits free electrons. Control of the display is achieved by the bias conditions placed on the grid and anodes. Column or character selection is provided through the grid while individual segment control is governed by the anodes. Electrons from the cathode or filament pass through a grid with a positive potential and are blocked by a grid with a negative potential applied. Electrons passing through the grid are attracted by anodes with positive potentials and are repelled by anodes with negative potentials applied (Figure 2). The applied voltages vary depending on the display format. Table I shows the range of element voltages and currents required by the majority of VFDs.

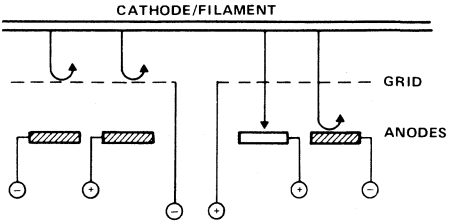


Figure 2. Vacuum Fluorescent Display Electron Flow

Table I. VFD Operating Ranges

Parameter	Min	Max
Cathode Voltage	2.4 V ac	10 V ac
Grid/Anode Voltages	24 V p-p	70 V p-p
Cathode Current	20 mA ac	250 mA ac
Grid Current	2.5 mA p-p	30 mA p-p
Anode Current	2.5 mA p-p	30 mA p-p
Power Dissipation	14 mW/Char.	125 mW/Char.

Panel Performance

Higher resolution VFDs pose problems. As higher resolution is pursued the mechanical and electrical properties of the VFD require special considerations. The grid is a fine screen mesh with practical limitations as to how small (or fine) it can be fabricated and handled. Additionally, as neighboring display elements are brought closer, magnetic fields created by their grids effect the display site being activated. The fringe field effect causes a nonuniformity in the luminance of the display. Most character displays employ a common grid for each character or column of characters. Thus the character spacing protects against this problem (Figure 3). Dot matrix displays, however, have no such space, thus a variation of grid/anode multiplexing is required. Figure 4 shows several arrangements of anode/grid connections used in dot matrix VFDs.

Except for the format shown in Figure 4(A), the configurations shown in Figure 4 provide good illumination. The particular style chosen depends on the application. Table II is the analyses of the total control pin count and cycle time required to complete one frame for various panel sizes.

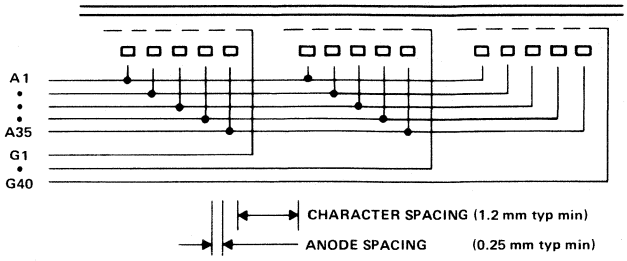


Figure 3. A 40: 5 × 7 Dot Character VFD

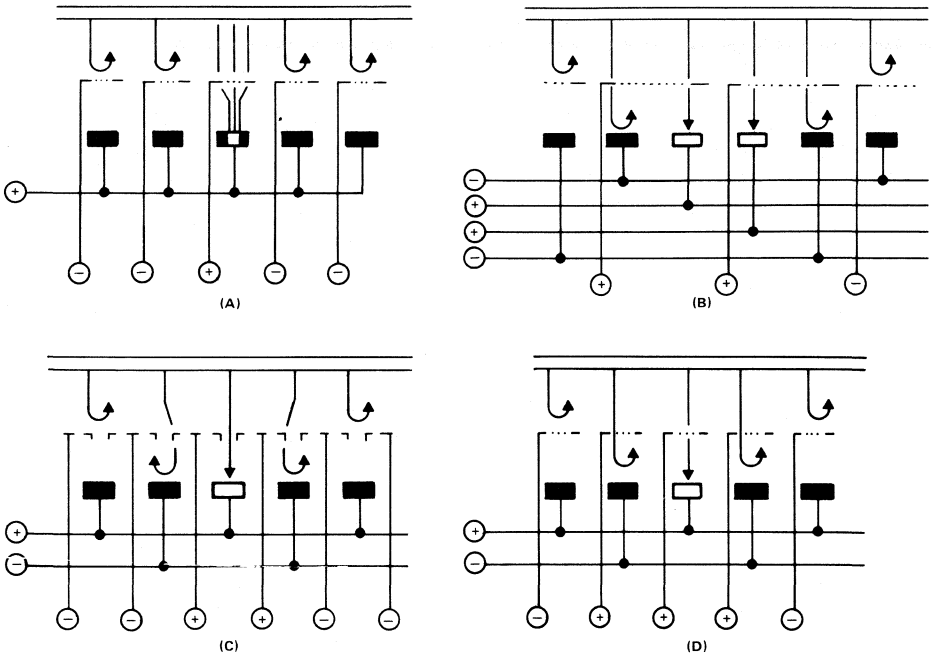


Figure 4. Grid-Anode Configurations of Dot Matrix VFDs

Table II. VFD Configuration Comparison

Parameter / Panel size / Config.	128 × 64				128 × 128				256 × 64			
	A	B	C	D	A	B	C	D	A	B	C	D
Anode Lines	64	256	128	128	128	512	256	256	64	256	128	128
Grid Lines	128	64	128	128	128	64	128	128	256	128	256	256
Total Lines	192	320	256	256	256	576	384	384	320	384	384	384
Cycles/Frame	128	64	128	128	128	64	128	128	256	128	256	256

VFD Timing Requirements

The VFD from a timing standpoint, is very forgiving. A typical cycle is shown in Figure 5.

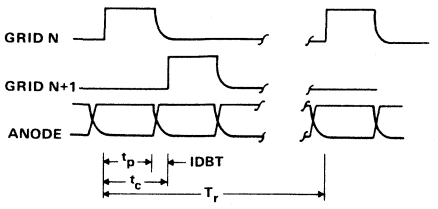


Figure 5. VFD Timing Diagram

The actual timing is governed largely by the application and panel size. The minimum panel refresh rate with undetectable flicker is 60 Hz. This defines the time (T_r) allotted to write the entire display one time (one frame) The amount of time allowed for each character or grid operation (T_c) is determined by the number of character or grid control lines (N) external to the display ($T_c = T_r/N$). To prevent noticeable degradation in the display intensity, each display site should be exercised at a minimum duty cycle of 1:150 ($T_p = T_r$/DUTY CYCLE). Neglecting any inter-digit-blanking (IDBT), a display could contain as many as 150 grid or character control lines. However, to prevent ghosts, some time must be allotted for inter-digit-blanking. The allowable dead-time between strobes (IDBT) is the difference between the character cycle time T_c and the character or grid strobe width T_p. As the number of grid or character control lines approach 150, the IDBT approaches zero (0). Conventional drivers with resistive pull-down require an IDBT as large as 30 μs (20 μs typically). Thus the maximum allowable number of grid or character control lines must realistically be less than 150. Most displays limit this parameter to 128 (a convenient binary number <150).

For a panel refresh rate of 100 Hz:
T_r = 10 ms
For an 80 character display
T_c = 10 ms/80 = 125 μs
For a 1:100 character duty cycle
T_p = 10 ms/100 = 100 μs
The allowable IDBT is;
IDBT = $T_c - T_p$ = 25 μs

Some applications may be limited by the excessive IDBT requirements of the resistive pull-down driver:
For a 128 grid display
$T_c = T_r/128$
For a 1:150 duty cycle operation
$T_p = T_r/150$
For a driver requiring 20 μs IDBT
IDBT = $T_c - T_p$ = 20 μs
T_r = 17.5 ms
The maximum panel refresh rate is:
$R = 1/T_r$ = 57 Hz (MARGINAL)

DRIVE ELECTRONICS

The following discussion on drive techniques will be limited primarily to the interface drivers on the display, their requirements and performance characteristics. Because the characteristics of the various display configurations change (see Figure 4), interface-driver circuit requirements differ. Texas Instruments offers an array of VFD drivers with a variety of features.

The UCN4810A

Figure 6 shows a block diagram of the UCN4810A. A Product Brief is included in the appendix of this report. The UCN4810A is a 10-bit active high VFD driver. Input data is stored in a 10-bit serial shift register on the positive transition of the clock. Parallel data is presented to the output buffers through a 10-bit parallel D-type latch. Data at the respective output of the shift register will be transferred through the 10-bit latch while the strobe input is high. Data present at the latches inputs during a negative transition of the strobe will be stored regardless of subsequent changes, providing the strobe input is low. A blanking control is provided which inhibits all output gates and assures they are low when the blanking input is high. All outputs are capable of sourcing 40 mA each from a V_{BB} supply voltage of 60 V, providing the maximum allowable package power limitation of 1.3 W is not exceeded. This limits the duty cycle of the on time for various load requirements (Table III). All inputs are CMOS compatible but require the addition of a pull-up resistor to V_{DD} when driven by standard TTL logic.

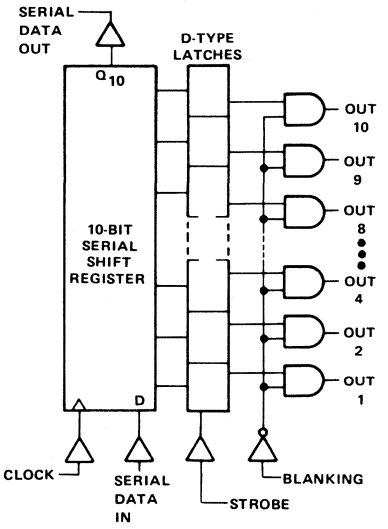


Figure 6. UCN4810 Functional Block Diagram

Table III. UCN4810A Operational Duty Cycle

Number of Outputs on I_O = 25 mA	Max. Allowable Duty Cycle at Ambient Temperature 25°C	40°C	50°C	60°C	70°C
10	100%	97%	85%	73%	62%
9	|	100	94	82	69
8	|	|	100	92	78
7	|	|	|	100	89
6	|	|	|	|	100
1	100	100	100	100	100

The TL4810A

The TL4810A is a substitute for the UCN4810A. A Product Brief of the 10-bit VFD driver is included in the appendix. The TL4810A utilizes an active totem-pole output to improve the sink current capability (2 mA vs 850 μA) without sacrificing the resulting power consumption as conventionally experienced in a passive pull-down structure. The totem-pole output is composed of an n-p-n emitter follower (source) and double-diffused MOS (DMOS) (sink) transistors. This improvement decreases the inter-digit-blanking time required and the overall device power consumption.

Unlike most VFD Drivers which are limited to an 85% duty cycle at 50°C, the TL4810A will sustain a 25 mA per output load at a 100% duty cycle over its entire operating temperature range of 70°C.

All device inputs are diode-clamped and compatible with standard MOS, CMOS and DMOS logic. Designed to control 10 VFD inputs, the TL4810A provides a positive edge triggered 10-bit serial shift register with a serial data out for serial transmission and registration of the display information. A 10-bit D-type latch accepts parallel data from the serial shift register when the strobe input is high. The data stored in the latch circuitry when the strobe input is taken low remains unaltered regardless of subsequent changes in the data present in the serial shift register. The latched information is then transferred to the output through the gated output buffers when the blanking output is low. A logic high on the blanking input causes all outputs to go low. All outputs are capable of sourcing 40 mA at 60 V.

The SN75512A

Figure 7 shows a block diagram of the SN75512A. A Product Brief is included in the appendix of this report. The SN75512 is a 12-bit VFD driver with totem-pole outputs. The active push-pull outputs minimize the required IDBT (<1 μs). Input data is stored in the 12-bit serial shift register on the positive transition of the clock input. Parallel data is presented to the output buffers through a 12-bit D-type latch. Data at the respective output of the serial shift register is transferred through the 12-bit latch while the latch input is high. Data present at the latches inputs during the negative transition of the latch is stored regardless of subsequent changes, providing the latch input remains low. The active-low strobe input enables all output gates. Each output is capable of sourcing 25 mA at a supply voltage of 60 V, providing the maximum package power dissipation of 1125 mW is not exceeded. Based on the maximum allowable voltage drop across the output at 25 mA sink current, the total package capabilities are as shown in Table IV. All inputs of the SN75512 are TTL compatible. A serial data-out is also available for cascading additional drivers.

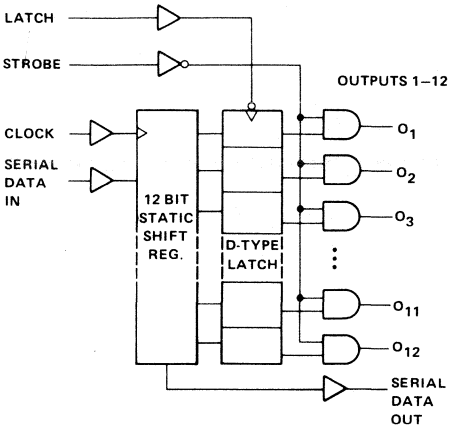


Figure 7. SN75512 Functional Block Diagram

Table IV. SN75512A–SN75513A Operational Duty Cycle

Number of Outputs on I_O = 25 mA	Max. Allowable Duty Cycle at Ambient Temperature 25°C	40°C	50°C	60°C	70°C
12	77%	68%	62%	55%	48%
11	84	75	67	60	52
10	92	82	74	66	58
9	100	91	82	73	61
8	|	100	93	83	73
7	|	|	100	94	82
6	|	|	|	100	96
5	|	|	|	|	100
1	100	100	100	100	100

The SN75513A

Figure 8 shows a logic diagram of the SN75513A. A Product Brief is included in the appendix of this report. The SN75513A is a 12-bit VFD driver with totem-pole outputs which minimize the required IDBT (<1 μs). Input data is shifted into a 12-bit serial shift register on the positive transition of the clock. Data appearing at the corresponding outputs of the shift register is presented directly to the output gates and is reflected at the output when the strobe input is low. Data in the shift register can be cleared with the reset input. A logic 0 on the reset input

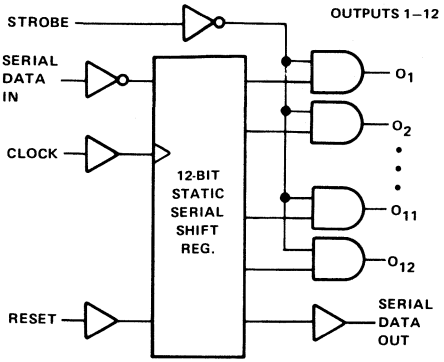


Figure 8. SN75513 Functional Block Diagram

clears the shift register contents to a logic 0. All outputs are capable of supplying 25 mA of source current at a V_{CC2} supply voltage of 60 V, providing the absolute maximum package power limitation of 1125 mW is not exceeded. Table IV reflects the derating resulting from this consideration. All input are TTL compatible and assume a logic high if left open. A serial data output allows cascading of several devices without additional circuitry.

The SN75501C

Although designed originally for AC Plasma applications, the SN75501C can be used to drive VFDs. The SN75501C is a 32-bit high-voltage display driver. A functional block diagram of the SN75501 is shown in Figure 9. For use as a VFD driver, the strobe input is grounded and the sustain input is operated as an active high strobe input. The 32-bit serial shift register, capable of

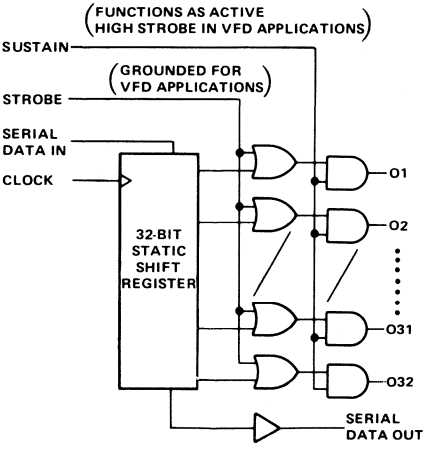


Figure 9. SN75501 Functional Block Diagram

4-MHz operation, registers the data on the positive edge of the clock. A logical "1" stored in the register will cause the respective output to pulse high when the sustain input is pulsed high. The outputs of the SN75501C are totem-pole outputs and a serial data out is provided for use in cascading multiple drivers. The use of the SN75501C as a VFD driver should be limited to applications where the dead time between strobe (sustain high) inputs is 74 μs or greater.

DISPLAY OPERATION

Driving a Vacuum Fluorescent Character Display

The following application uses a 5 X 7 40-digit VFD by Noritake. Each character is written in a single cycle since all 35 anodes (A1 through A35) of the 5 X 7 matrix are pinned out. The characters (1 through 40) are scanned by selective control of their respective grid, each of which is pinned out (G1 through G40). Respective anodes of all characters (A1 of Char 1 through Char 40) are connected. This format is common to most dot character or segment character displays (Figure 10). Multirow displays require additional control. This is usually provided through parallel access to the anodes of each additional row (Table V).

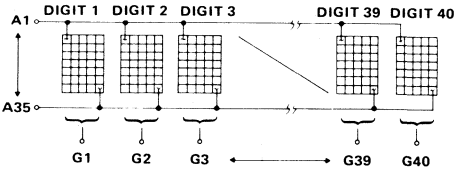


Figure 10. A 40: 5 X 7 Dot Character VFD Configuration

Table V. Dot Character VFD Driver Requirements

Control Pins					Required Drivers	
Anode	Grid	Rows	Char	Matrix	10 Bit	12 Bit
35	10	1	10	5 X 7	5	4
	40		40	5 X 7	8	7
60	10		10	5 X 12	7	6
	40		40	5 X 12	10	9
70	10	2	10	5 X 7	8	7
	40		40	5 X 7	11	10
140	10	4	10	5 X 7	15	13
	40		40	5 X 7	18	16
210	10	6	10	5 X 7	22	19
	40		40	5 X 7	25	22

A typical driver scheme for a single line 40:5 X 7 dot character VFD is shown in Figure 11.

Whether or not the anode drivers require latched outputs depends on the circuit timing. Figure 12 shows a typical timing diagram for the display as shown in Figure 11.

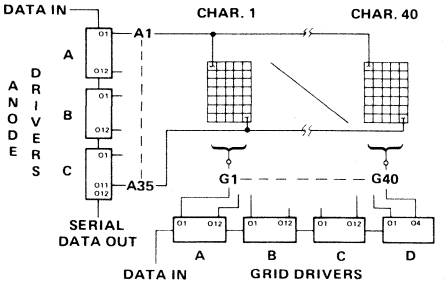


Figure 11. A 40: 5 X 7 Dot Character VFD Drive Scheme

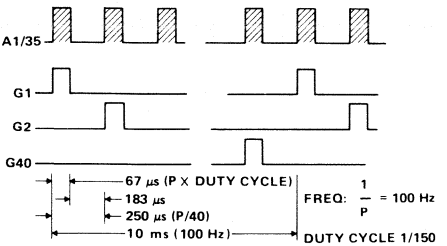


Figure 12. A 40 Character VFD Timing Diagram

The drivers remain inactive for 183 μs prior to each character registration. This is more than sufficient time to load the 35 bits of data required for each character. With a 1-MHz data rate, the SN75513A requires only 35 μs to load this information. Modification of the timing to take advantage of the latch capability of the SN75512A for this particular application (1 line – 40:5 X 7 character VFD) will produce questionable improvement in display aesthetics. This is not the case for larger displays. Take for example, a six-line display of similar format (Table V). A six-line display (DC40066A) requires control of 210 anodes (6 X 5 X 7). Thus unless received in parallel format, this requires 210 μs loading time. With a latched driver however, this presents no problem as new data can be entered independent of the IDBT. Figure 13 illustrates a typical timing diagram incorporating this design.

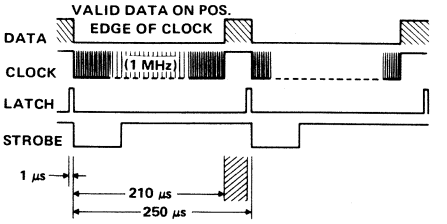


Figure 13. Data Registration of a SN75512 12-Bit VFD with Latch

The latch function virtually extends the time allotted for data registration in the anode drivers to the full character cycle time. For a 100-Hz panel refresh rate and 1.150 minimum character duty cycle, the minimum character cycle time is 67 μs. The larger the panel the more complex the anode/grid configuration, the more beneficial the latch feature (as that available with the SN75512) becomes.

Driving a Dot Matrix Display

As discussed in a preceding section on Panel Performance, several variations of grid/anode configurations exist. The following will present the panel requirements and suggested drive techniques for the displays shown in Figures 4(B), 4(C), and 4(D).

Figure 14 illustrates the VFD grid/anode arrangement for a DM 256 X 64A. This is a 256 X 64 dot matrix VFD by Noritake whose grid/anode configuration is as illustrated in Figure 4(B). Figure 15 shows the required timing of the anode and grid signals to properly operate the DM 256 X 64A. As can be seen in Figures 14 and 15, the active columns are composed of anodes which are in-board the activated grids. When grids 1 and 2 are activated, columns 2 and 3 are in-board, and columns 1 and 4 are out-board. The purpose of this arrangement is to eliminate fringing effects of neighboring grids and thus achieve uniform intensity. Analysis of this configuration also shows requirements on panel drive electronics which are common to the previous examples. If the total panel refresh rate is held to 100 Hz, the total panel period (T) is 10 ms. With 128 write cycles required, each write cycle is 78 μs. Maintaining the 1:150 duty cycle, each strobe signal is 66 μs. This allows only 12 μs dead time or IDBT which dictates the use of an active pull-down driver. The time between the strobe signals of a particular anode group is 90 μs. This opens several options in the VFD driver architecture. Each group of anode drivers requires 64 bits of data and two groups (A & D or B & C) must be loaded during each column write cycle (128 bits). If the SN75512 is used, its latch feature allows use of total strobe cycle period (156 μs), and a 1-MHz data rate allows the data to be received in a serial format. If the SN75513A is used, the A(B) group and D(C) group data must be loaded in parallel (64 μs), since it must be loaded during the dead time between strobe signals. Also available is the SN75501. Since the strobe signal duty cycle is less than 50%, the SN75501 can also be used. With a 4-MHz data rate, all 128 bits of data can be registered serially in the 32 μs dead time between strobes.

Figures 16 through 19 illustrate the dot matrix pinout and timing diagrams for the anode/grid configurations shown in Figure 4(C) and 4(D). Table VI identifies applicable anode and grid drivers and the number required for each of the configurations presented.

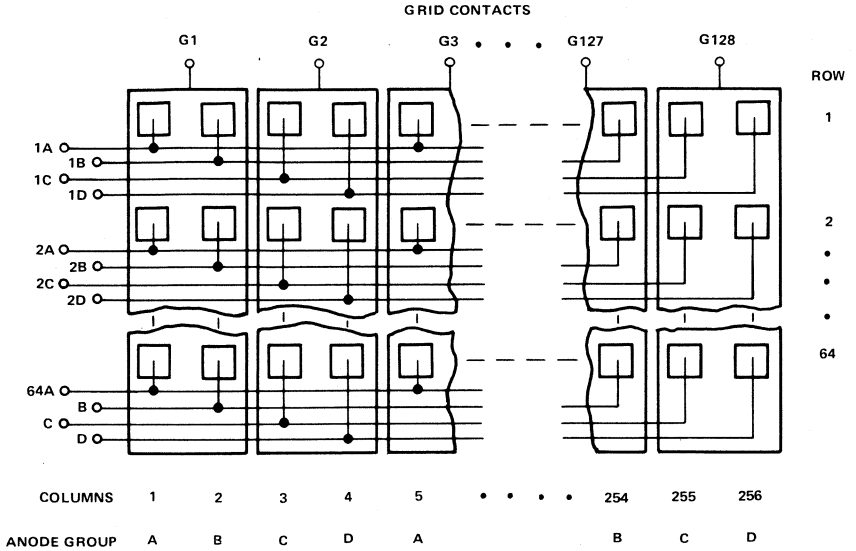


Figure 14. A 256 X 64 Dot Matrix VFD Pinout

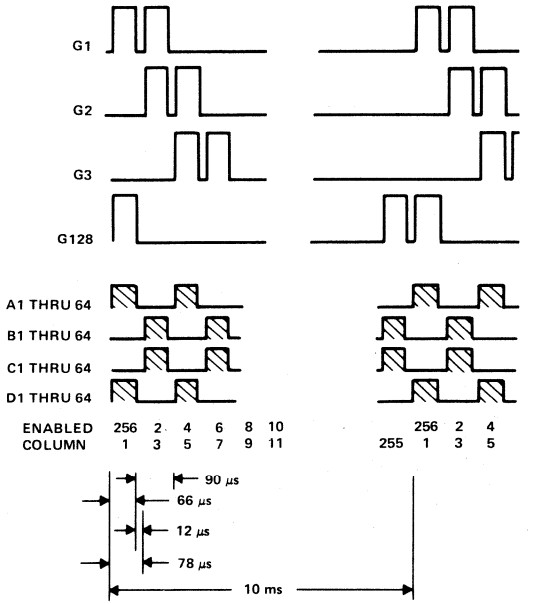


Figure 15. Timing Diagram for VFD of SN75512

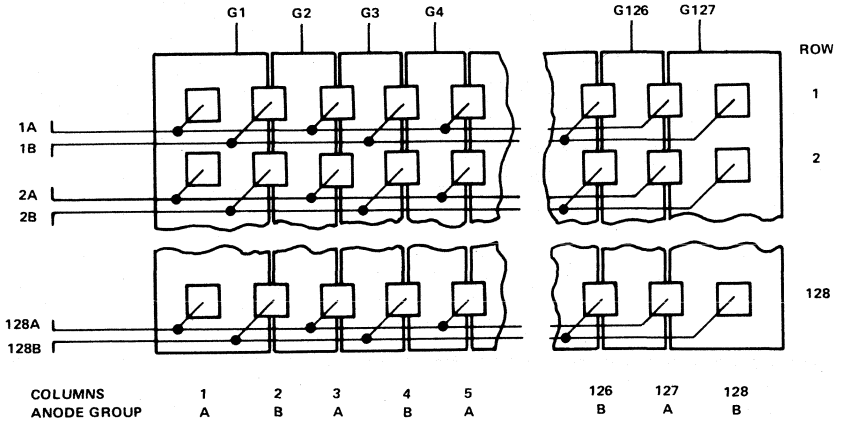


Figure 16. A 128 X 128 Dot Matrix VFD Pinout

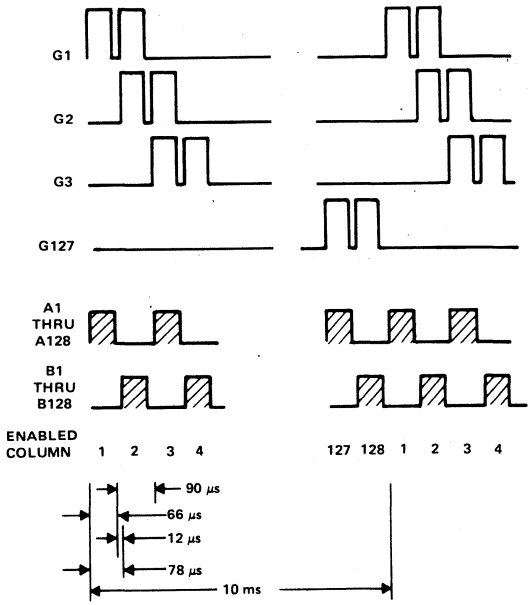


Figure 17. Timing Diagram for VFD 128 X 128 Dot Matrix

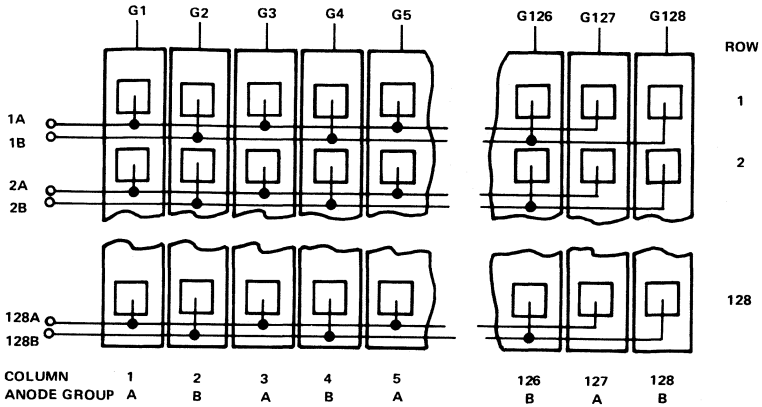


Figure 18. 128 X 128 Dot Matrix VFD Pinout

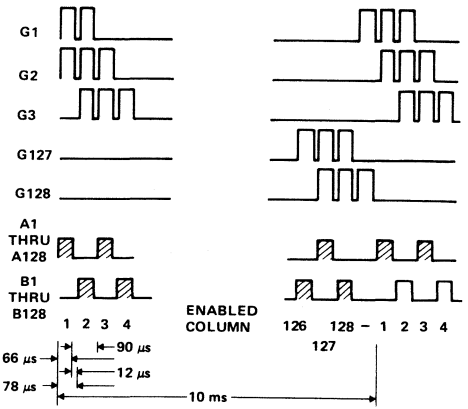


Figure 19. Timing Diagram for VFD of 128 X 128 Dot Matrix Pinout

Table VI. Dot Matrix VFD Driver Requirements

Display Size	Format	Control Lines		No. Drivers Required			
		Anode	Grid	4810	512	513	501
128 X 64	Fig 14	256	64	26+7	22+6	24+6	8+2
	Fig 16	128	128	14+13	12+11	12+11	4+4
	Fig 18	128	128	14+13	12+11	12+11	4+4
128 X 128	Fig 14	512	64	52+7	44+6	NA 6	16+2
	Fig 16	256	128	26+13	22+11	NA 11	8+4
	Fig 18	256	128	26+13	22+11	NA 11	8+4
256 X 64	Fig 14	256	128	26+13	22+11	24+11	8+4
	Fig 16	128	256	14+26	12+22	12+22	4+8
	Fig 18	128	256	14+26	12+22	12+22	4+8

AC Plasma Display

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INTRODUCTION

The persistent interest in flat panel information displays has stimulated the continual development of the gas discharge display. Their thickness, durability and screen size have been the primary advantages over conventional display technologies. The following report outlines the construction and application of the AC Plasma Display.

THE AC PLASMA DISPLAY

The AC Plasma Display is an X-Y matrix gas discharge display. The basic display element is the gas discharge that occurs at the intersection of selected electrodes when the applied voltage between the electrodes exceeds the breakdown voltage of the media gas with which the display is filled. When the breakdown voltage of the gas is exceeded, the gas is ionized and the discharge that occurs emits a visible spot of light at the intersection of the selected electrodes. Once initiated, the display element can be maintained active without further selective control. The data retention property of the ac plasma display eliminates the necessity of a memory map for simple information displays.

Construction

The simple construction techniques employed are another feature encouraging the development of the ac plasma display panel. The panel envelope is essentially two flat pieces of ordinary glass spaced apart and sealed around the peripheral edges as shown in Figure 1.

The electrodes are deposited on the internal surfaces of the glass plates and then covered by an insulating dielectric layer prior to their joining. The space between the glass plates is evacuated and filled with a media gas under low pressure (approximately one-fifth atm). Unlike the dc plasma display panel where the electrodes are immersed in the media gas, the electrodes of the ac plasma panel are isolated from the media gas by the dielectric layer. This dictates ac operation utilizing the capacitive coupling of the insulated ac plasma display cell.

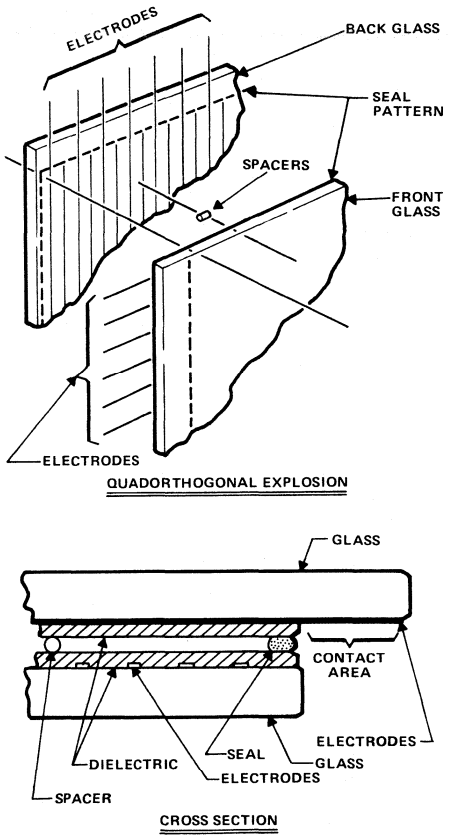


Figure 1. Panel Construction

Early panels utilized a third piece of perforated glass, which defined the individual display cell or pixel. Current panels, however, use an open-cell structure which eliminates the masking glass. Individual cells thus constructed are defined by properly ratioed media gas pressure, electrode width and resolution, glass spacing, and excitation and sustaining potentials. ***Individual cells*** are defined as the area located at the intersection of the mutually perpendicular electrodes of the front and back plates. The parallel electrodes of each plate of the panel are usually divided, every other electrode exiting from opposing edges of the plate, to allow easier access for the mechanical interface required to connect the electrodes to the control circuitry. The simple construction of the ac plasma panel yields a rugged sandwich containing only a few cubic centimeters of inert gas. There is no danger of implosion as found with conventional vacuum tube displays, and no danger of contact with high voltages through the glass faceplate. To say nothing of the achievable cost of the ac plasma display panel, the construction techniques yield one of the safest display panels in today's marketplace.

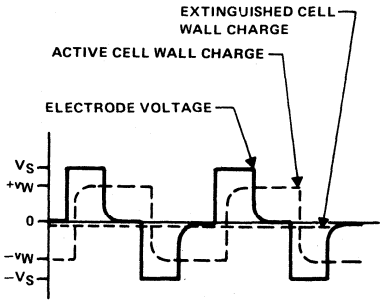


Figure 2. Cell Waveforms

The Functional Cell

Light is emitted from the ac plasma cell as a result of the discharge that occurs when the media gas is ionized. This is accomplished by simply applying sufficient potential across the cell to break down the media gas. Since the actual cell is only capacitively coupled to the electrode potential, voltage waveform, frequency and amplitude are interdependent to reliable plasma display operation.

When ionization of the gas occurs, a charge buildup is created by the high electron and ion currents present in the ionization discharge sequence. This charge buildup, or ***wall charge*** as it is commonly identified, plays an important role in the ability of the ac plasma panel to maintain display information without further selective control. Figure 2 shows a typical applied ac waveform and the wall charge waveforms of an active and extinguished cell. These relationships are observed at all cell locations during that period of time in which no panel information is being altered (written or erased). This is normally identified as the ***sustain mode***.

A typical write-sustain cycle waveform is shown in Figure 3. The electrode potential and resulting wall charge are plotted to show their interdependence in writing (initializing) and sustaining a selected cell.

Prior to the cycle in which the selected cell will be written, the cell being exercised exhibits zero wall charge. Therefore, the potential seen by the cell (the **cell voltage**) is solely the potential applied to the electrodes (the **electrode voltage**). When the electrode voltage exceeds the breakdown voltage of the media gas, the gas ionizes and the wall charge is deposited such that its polarity opposes the applied cell voltage. Once created, the wall charge remains even after the ionization discharge extinguishes and the electrode potential decays to zero. In the next half-cycle, the electrode potential reverses, thus the wall charge that opposed the electrode voltage in the previous half-cycle now is additive. The cell voltage is therefore the sum of the wall voltage and the electrode voltage. This allows the electrode voltage to be reduced and still create a cell voltage of sufficient amplitude to cause the cell to fire. Stable operation exists when the sum of the electrode potential and wall charge create a cell voltage (V_{W2}) which is sufficient to create ample excess charge ($2\ v_W$) to cause the wall voltage to invert. Thus the cell can be maintained indefinitely by an alternating electrode potential which is actually less than the potential required to fire the cell. The ability to do this is attributed chiefly to the nonlinear charge transfer characteristics of the ac plasma cell, as illustrated in Figure 4. Since the sustaining electrode potential is less than the required firing potential of the extinguished cell, application of this voltage will have no effect on cells which have not been fired previously. With this in mind, operation of the ac plasma display is relatively simple. A background signal is applied to the entire display panel indiscriminately. This is usually called the ***sustain signal***. Select circuitry superimposes the pulse required to initially fire a cell on the X and Y-axis electrodes common to the cell to be written into. Once fired, the background signal will maintain the integrity of a cell until the cell is extinguished by another selective control signal, normally called the ***erase pulse***. This is accomplished by application of a signal to the cell electrodes whose amplitude (V_{W1}) and duration are only sufficient to create enough excess charge to counterbalance the wall charge. Thus the wall charge is removed and the sustain chain sequence is broken. An illustration of this operation is shown in Figure 5.

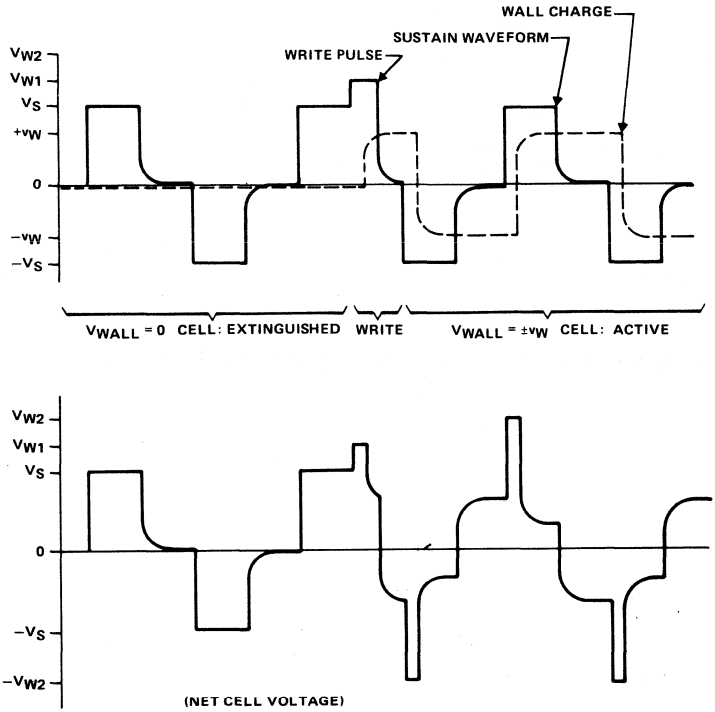


Figure 3. Write-Sustain Cycle Cell Waveforms

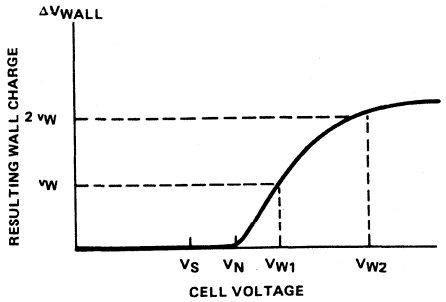


Figure 4. Charge Transfer Characteristics of AC Plasma Cell

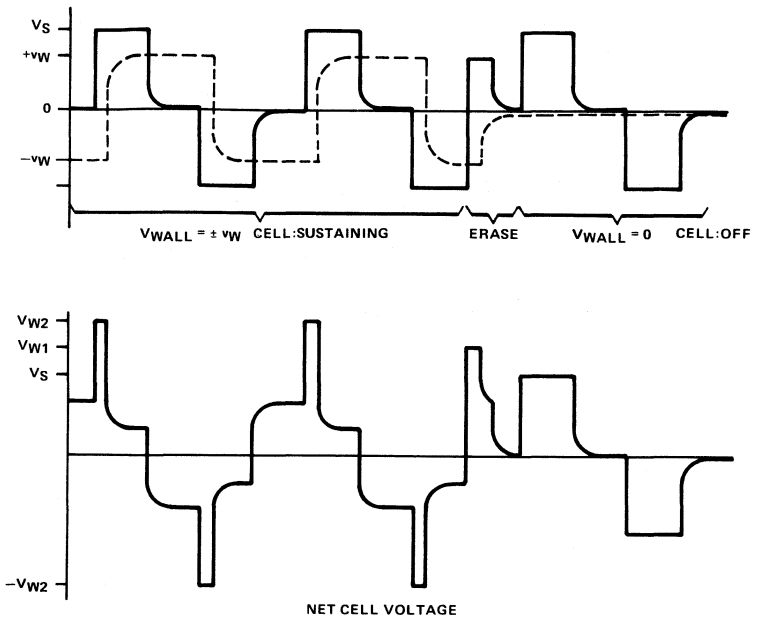


Figure 5. Sustain-Erase Cycle Cell Waveforms

The Control Circuitry

Actual circuitry may vary based on the specific application being addressed so long as the net result, the differential electrode potential waveforms, yields reliable control. One such approach utilizes the principle of the H-Bridge. This reduces the requirements on the power supply and enables the two drivers to share in the generation of the functional waveforms. Additional approaches will be presented primarily to illustrate the variety of acceptable drive schemes.

The drivers used in these approaches are the SN75500A and SN75501A ac plasma display drivers from Texas Instruments. Designed specifically for ac plasma display applications, the SN75500A and SN75501A mark a significant milestone in the development of the ac plasma display technology. Prior to their development, the high voltage requirements of the plasma panel prevented the use of conventional integrated circuits as electrode drivers. This meant that the electrode interface must employ discrete components for proper control. This is quite prohibitive on larger panels without a more sophisticated drive scheme. The SN75500A and SN75501A drivers each provide circuitry required for active control of 32 electrodes. Interface to a 256 line by 256 line panel can now be achieved with a total of 16 integrated circuits (eight SN75500A and eight SN75501A). Use of these devices allows a significant reduction in the complexity and cost of the system electronics required to operate the ac plasma display.

The Functional Waveforms

The functional waveforms developed are the primary waveforms which provide the basic functions required in the operation of an ac plasma panel display: sustain, write, erase and blanking. These waveforms are only one of several approaches, all of which may provide satisfactory operation. The main intent of this application report is to present the methods used to develop the waveforms and the implementation of the SN75500A and SN75501A drivers.

Figure 6(A) illustrates the basic waveforms for write, sustain, erase and blanking. This is the net differential waveform created between the X and Y-axis electrodes by excursions on the X-axis or Y-axis or both. Figure 6(B) shows the composition of the differential waveform and identifies the origin of the components.

The first sequence of waveforms to consider is the sustain waveform. Review of Figure 6 shows the sustain waveform to be composed of two parts: the base pulse applied to the X-axis and a negative excursion on the Y-axis. It is important to note that this basic waveform is found in all other waveforms which require the retention of the panel data (selective write, selective erase). Additionally,

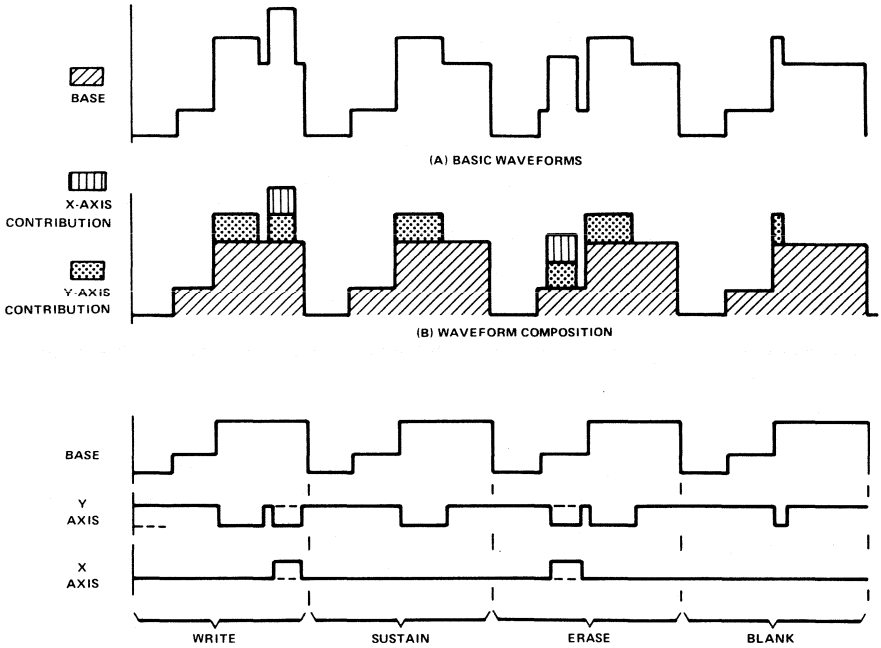


Figure 6. Functional Waveforms

this signal is nonselective, it must appear at all electrode nodes where the cell data is to be maintained. Any cell not experiencing this differential signal will fail to retain its active status. The first component of the sustain waveform, the base pulse, is generated external of the X-axis drivers, and is applied to all electrodes addressed along the X-axis. Thus it is identified as the ***X-axis sustain***. Additionally, since the drive for all the X-axis electrodes share common circuitry, the X-axis sustain is commonly called the ***bulk sustain***. The second component of the sustain waveform, the negative pulse appearing on the Y-axis is not considered a bulk sustain signal since it is created by the Y-axis drivers and each electrode addressed along the Y-axis is driven by its associated driver output circuitry. Supplemental pulses thus created are identified with their axis, ***Y-axis sustain***. Together, the ***bulk (X-axis) sustain*** minus the ***Y-axis sustain*** combine to compose the basic ***sustain*** waveform. The SN75501A AC Plasma Driver was specifically designed to provide the Y-axis driver function. Additional control of the output circuitry allows all outputs (32) to be switched low, independent of the select control circuitry employed in selective output operations such as write and erase. All the outputs of the SN75501A switch low when the sustain input is taken low, thus all electrodes addressed along the Y-axis experience the Y-axis sustain signal. The blanking waveform is also a nonselective waveform as it is used to blank the entire panel. Composed of the same components as the basic sustain waveform, it is similarly created.

The write and erase operations are selective operations. In other words, the pedestals superimposed on the basic sustain waveform, which create the write and erase waveforms, appear only at the pixels (electrode intersections) whose information is to be altered. This is accomplished by superimposing half the required pedestal on each of the associated X and Y-axis electrodes. This is illustrated in Figure 7.

All other nodes experience either a standard sustain waveform or a ***half-select*** waveform. Standard sustain waveforms appear at all nodes where neither of the associated electrodes (X-axis or Y-axis) exhibit a half-select pulse. A half-select waveform appears at all nodes where only one of the associated electrodes exhibits a half-select pulse. The pedestal created by a single electrode excursion in a half-select waveform is insufficient to ionize the media gas and initiate a write-sustain sequence. The half-select pulses appearing on the X and Y-axis are created by the X and Y-axis drivers respectively. The SN75500A X-axis and SN75501A Y-axis drivers are designed to provide these functions. Both devices contain circuitry for selective

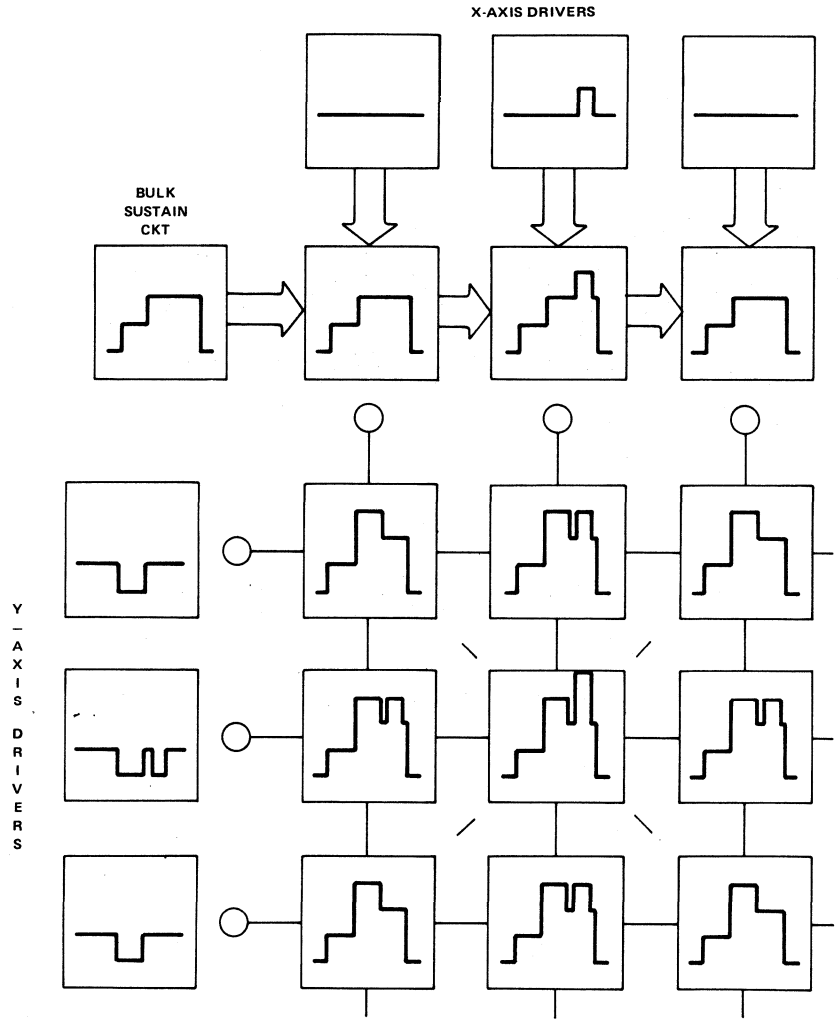


Figure 7. Write Waveform Array and Origin

control of their outputs. The specifics of this circuitry are discussed in their respective sections. Let it be sufficient to say at this time, that with proper data controls established, the selected outputs of the SN75500A switch positive and the selected outputs of the SN75501A switch negative when the strobe input of both devices is pulled low. The determination of a write or erase operation depends on the timing of the strobe. Figure 8 illustrates use of the sustain and strobe inputs in the generation of the basic operational waveforms.

As mentioned previously, a variety of approaches for driving the AC Plasma panel can be employed. The previous approach utilized the half-select principle for selective operations with an X-axis bulk sustain and a Y-axis supplemental sustain. Additionally, the X-axis drivers floated on the bulk sustain signal while the Y-axis drivers remained ground based. The following example incorporates split sustain and uses a common driver for both axis. Selective operations are performed using the blanking principle.

A split axis sustain merely says both axes employ an externally generated bulk sustain signal. Figure 9 illustrates how the basic sustain waveform is created using this approach. The blanking technique for selective operations superimposes a full-select pedestal on one axis (X-axis). Locations along the selected electrode which are not to be altered are then canceled by a blanking pulse of like amplitude and polarity applied to the intersecting (Y-axis) electrode at that location. Since both axes require a selective pulse of the same polarity, a common driver is used for both axes. Figure 10 illustrates the array of waveforms created using this approach and their origin.

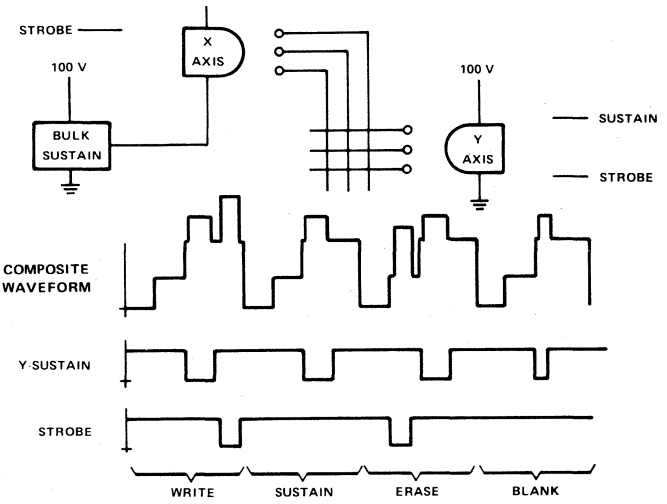


Figure 8. Control Signal Timing

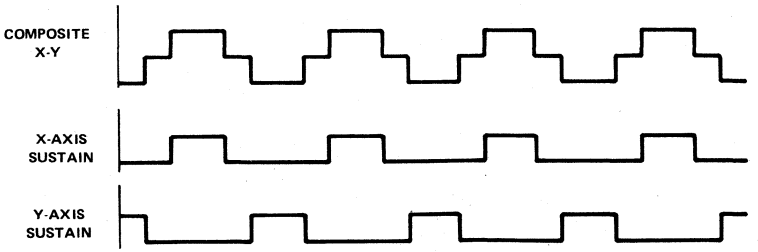


Figure 9. Split Axis Sustain

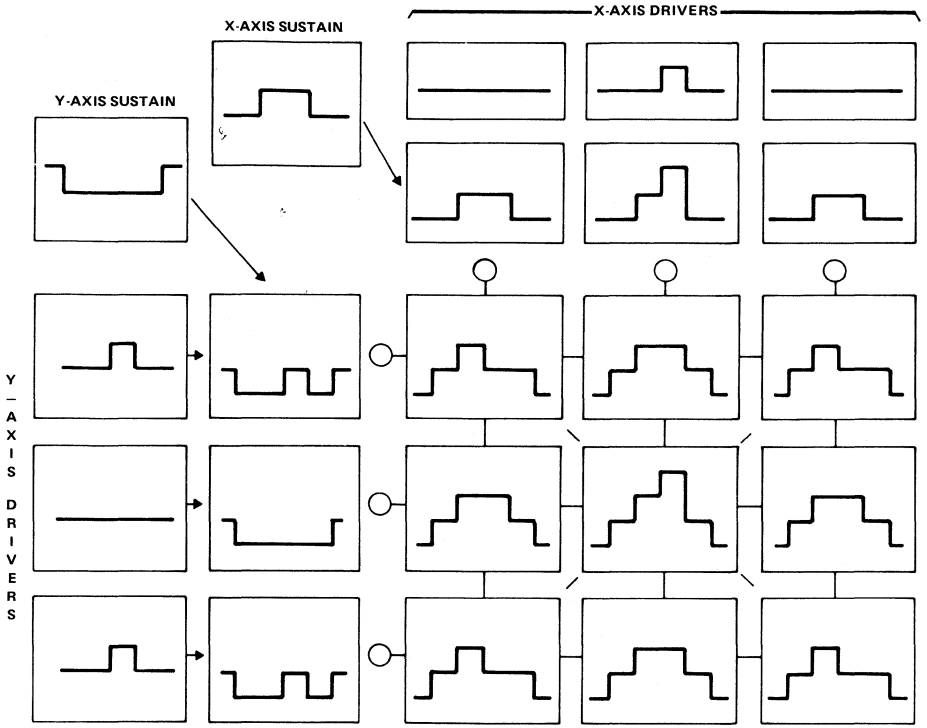


Figure 10. Write Waveform Array and Origin
Split Axis Sustain – Blanking Select

SN75500A AC PLASMA DISPLAY X-AXIS DRIVER

The association of the SN75500A driver to the X-axis is misleading. The operation of the SN75500A on the horizontal or vertical electrodes is primarily dependent on the panel's application. The outputs of the SN75500A are normally low and switch high selectively when the strobe input is low. The SN75500A thus provides the positive select pulse. A functional block diagram of the SN75500A is shown in Figure 11. Selection of the outputs (32) is accomplished with the select and data inputs. The 32 outputs of the SN75500A are divided into four sections (1QX, 2QX, 3QX, 4QX) of eight outputs each. Only one of the four sections can be activated at one time (eight outputs). All other outputs (24) remain low. For this reason most systems use the SN75500A to scan the electrodes along which the information is written. Selection of the specific section is determined by the select inputs S0 and S1 (Table I). When selected, the state of the eight outputs of the section is determined by the data stored in the 8-bit storage register. Data is shifted into the storage register in a serial fashion on the positive transition of the clock. The maximum guaranteed data rate is 4 MHz and the strobe input must be held to a logic 1 level during the data entering period. Data is shifted into the Q1 register and progresses to the Q8 register. A logic zero entered at the serial data input selects the outputs which will switch high when the SN75500A is strobed (pulsed low). All outputs of the SN75500A contain clamp diodes to the V_{CC2} and GND supply inputs. These diodes play an important role in the functional adaptation of the SN75500A. The specifics of which are discussed in the following section on the Functional Adaptation of the SN75500A and SN75501A. Push-pull circuitry on each output provides active switching between the GND and V_{CC2} supplies. All inputs of the SN75500A are CMOS compatible ($V_{TH} \approx 5$ V) and assume a logical 1 if left open. A typical operating sequence is shown in Figure 12.

Table I. Select Input Truth Table

S0	S1	Outputs Enabled
0	0	1Q1 thru 1Q8
1	0	2Q1 thru 2Q8
0	1	3Q1 thru 3Q8
1	1	4Q1 thru 4Q8

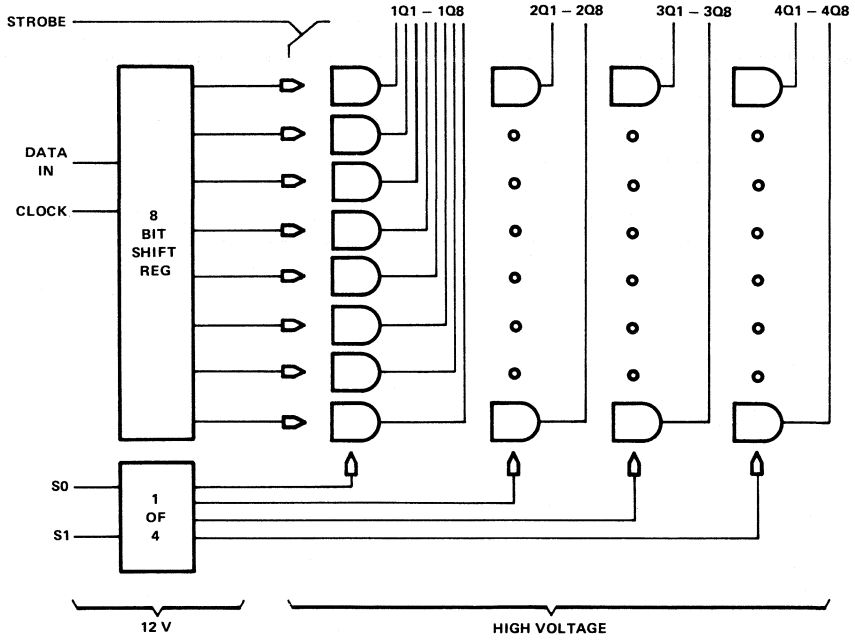


Figure 11. SN75500A Functional Block Diagram

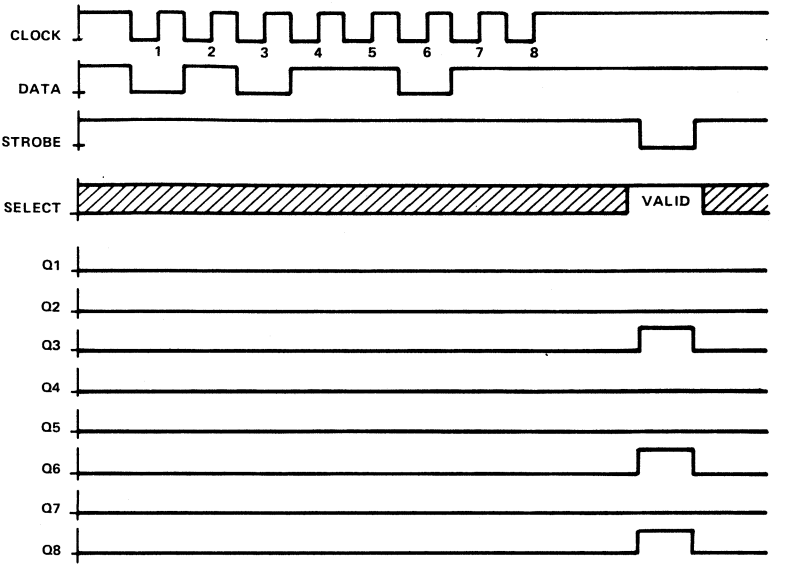


Figure 12. Typical Operating Sequence – SN75500A

SN75501A AC PLASMA DISPLAY Y-AXIS DRIVER

As with the SN75500A, the association of the SN75501A with the Y-axis is misleading. The SN75501A is designed to generate the negative select pulse. In addition, the internal control circuitry provides for all outputs to be switched low independent of the stored data when the sustain input is taken low. This feature is provided primarily for the purpose of creating a supplemental sustain signal. Unlike the SN75500A, the SN75501A can operate on all 32 of its outputs at one time. A functional block diagram of the SN75501A is shown in Figure 13. Control of the output gates is established in the internal 32-bit shift register. A logic zero at the serial data input selects the outputs which will switch low when the strobe input is taken low. Data enters the serial shift register on the positive transition of the clock input. The maximum data rate is 4 MHz and the strobe and sustain inputs must be held to a logical 1 during the period data is being entered. All outputs of the SN75501A contain clamp diodes, the V_{CC2} and GND supply terminals. This allows it to be operated on a base waveform where required. The push-pull output circuitry provides positive switching of all outputs between the V_{CC2} and GND supplies. The CMOS compatible inputs ($V_{TH} \approx 5$ V) assume a logical 1 if left open. A typical operating sequence is shown in Figure 14.

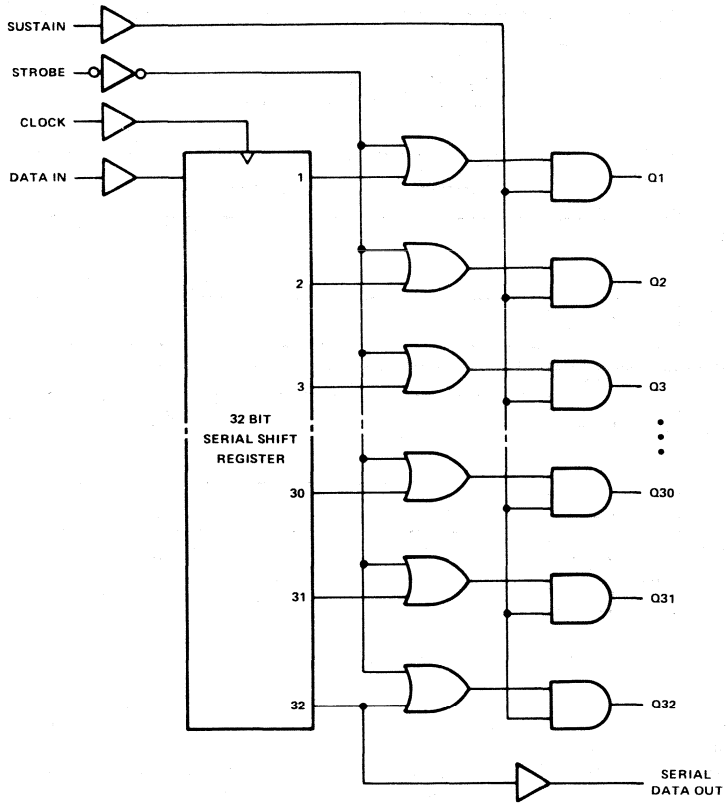


Figure 13. SN75501 Functional Block Diagram

FUNCTIONAL ADAPTATION OF THE SN75500A AND SN75501A

In the previous text, functional waveforms were discussed. It is the intent of this section to discuss the adaptation of the SN75500A and SN75501A to these drive techniques and to identify specific conderations which must be observed for satisfactory operation.

Strobing and Sustaining

The output gate circuitry for the SN75500A and SN75501A is virtually identical. Both devices contain a pair of DMOS output transistors for active control of the output. The lower DMOS transistor receives its drive from the low voltage supply, V_{CC1} (12 V). Thus the power consumption of the gate drive cricuitry is minimal. The gate drive of the upper DMOS structure however experiences the full high voltage bias (100 V). To minimize its power dissipation, the gate circuitry incorporates a dynamic drive scheme which coincides with the dynamic output current requirements of the panel. In other words, the drive circuitry initially provides a large gate current capable of saturating the upper DMOS transistor during the transition period of the output when the current demand is large. As the panel capacitance is charged and the current requirements decrease, so does the gate drive. This kick current occurs every time the output of the drivers is required to switch high.

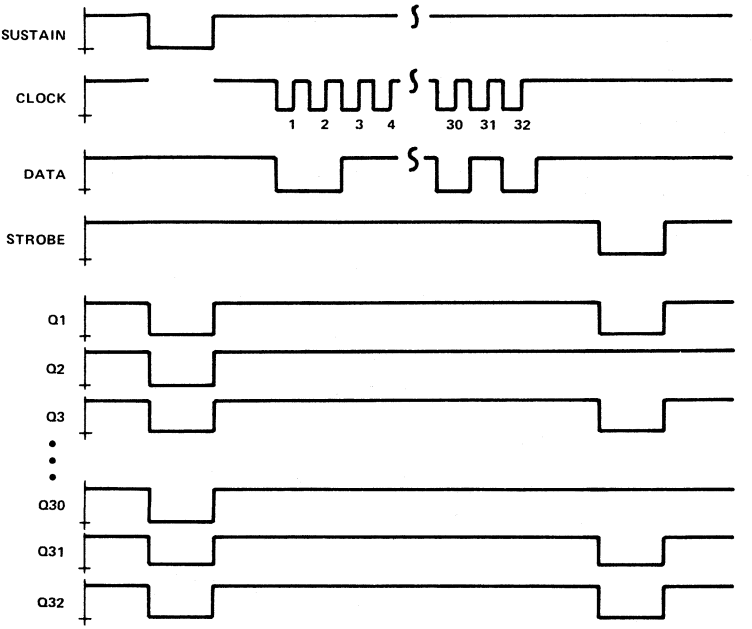


Figure 14. Typical Operating Sequence – SN75501A

The kick current is approximately 60 mA with a duration of 2 microseconds. If operated in a system whose V_{CC2} is 100 volts, the resulting power consumption is 12 microjoules. The average power dissipation then depends on the frequency at which the kick circuit is employed. In a system operating at a 50 kHz (period = 20 micorseconds), this equates to an average dc power of 600 mW.

$$\frac{60\text{ mA} \times 2\ \mu\text{s} \times 100\text{ V}}{20\ \mu\text{s}} = 0.6\text{ W}$$

This represents a 45°C rise in the chip temperature over the ambient. The kick circuit being discussed here is activated every time the output is strobed regardless of whether or not the data causes the output to switch. For this reason, a selective strobe architecture is preferable in a system that updates panel information every cycle. Thus, each driver experiences only the additional power dissipation while it is actively performing the panel operations (writing or erasing) thus reducing the duty cycle and effective dc power. In a 512 line panel (16 drivers: 8/side), this represents an 88% reduction in power due to data operations. Panels which fill an entire line or column with data to be written in parallel also reduce the effective dc power. With a maximum data rate of 4 MHz, it requires 64 μs to enter 256 serial data bits (8 drivers × 32 bits). If the information is then written on the panel in the fifth cycle, the effective power resulting from the data operations on the panel is reduced by 80%.

These strobing techniques affect only the kick circuit power associated with the data operations of the devices. In the case of the SN75500A, this is its only contribution. With the SN75501A, however, the kick circuit not only applies to strobed response of the driver but also to the sustain response. If the sustain feature of the SN75501A is employed as in the initial example, the SN75501A output is pulsed twice in each cycle and the average power increases to 1.2 W.

$$\frac{60\text{ mA} \times 2\ \mu\text{s} \times 100\text{ V}}{20\ \mu\text{s}} \times 2 = 1.2\text{ W}$$

This constitutes a 90°C rise in the chip temperature over the ambient. Depending on the application (frequency, V_{CC2}, strobe technique), it may be more desirable to perform the sustain function external of the SN75501A. At this time (October 1980), improvements in the kick circuit are being implemented which will alleviate this problem by reducing its contribution to the overall power consumption by 80%.

FLOATING DRIVER CONSIDERATIONS

In most applications, one or both axis drivers will be required to operate (float) on a base waveform. Output clamp diodes have been provided on each output to accommodate this requirement. Figure 15 shows the output structure which is common to both driver circuits, SN75500A and SN75501A.

In the case of the SN75501A, the output is normally high, therefore Q1 is normally on. A base pulse applied to the SN75501A is therefore applied to the V_{CC2} terminal. As shown in Figure 16, positive excursions on the V_{CC2} terminal are passed through the output transistor Q1 while negative excursions are coupled through the catch diode D1. Since the data retention and decode circuitry receive their bias from the V_{CC1} supply (12 V), variations in the V_{CC2} supply will be reflected at all outputs but will not affect the stored data present in the SN75501A's register. If the outputs of the SN75501A are not required to switch below ground, the SN75501A may be operated ground-based even though the V_{CC2} incorporates a base signal. Figure 17 illustrates a typical application which behaves in this manner. The only limitations are:

1. V_{CC2} must never be less than GND or greater than 100 volts above GND (GND $\leq V_{CC2} \leq$ 100 V)
2. The strobed data pulse occurs while V_{CC2} is at any potential other than GND ($V_{CC2} \neq$ 0 V)
3. The strobed data output pulse is always required to switch to 0 volts (GND).

If the data pulse is required to occur at various levels on the base pulse or switch to a potential other than GND (0 V), the SN75501A must float with the base pulse waveform. This can be accomplished with floating V_{CC2} and V_{CC1} supplies referenced to the base waveform or by utilizing a capacitive storage bridge like that shown in Figure 18.

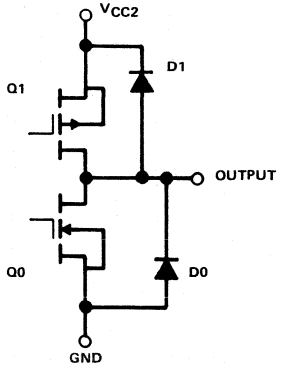


Figure 15. SN75500A and SN75501A Output Structure

The SN75500A output is normally low, thus the output transistor Q0 of Figure 15 is normally on. A base pulse applied to the SN75500A is therefore applied to the GND terminal. As shown in Figure 19, negative excursions on the GND terminal are passed through the output transistor Q0 while positive excursions are coupled through the catch diode D0. When utilizing this feature of the SN75500A, caution must be taken to assure proper retention of the data and to prevent excessive power consumption. When the lower clamp diode D0 is forward biased as is the case during the positive transition of the GND terminal, the SN75500A substrate also becomes forward biased. In this condition the output current demand is supplied in part from the high-voltage supply. Even though the current is

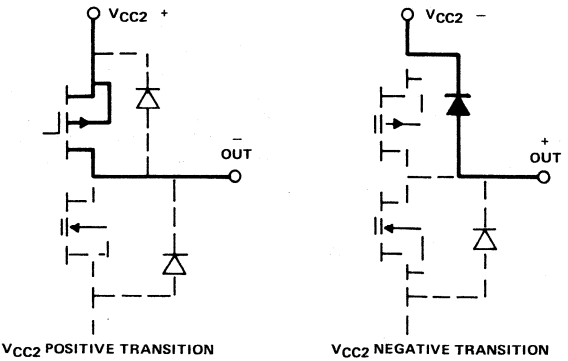


Figure 16. Floating SN75501A Current Paths

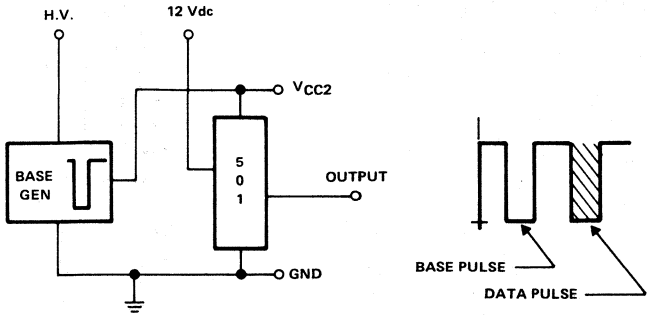


Figure 17. SN75501A with Pulsed V_{CC2}

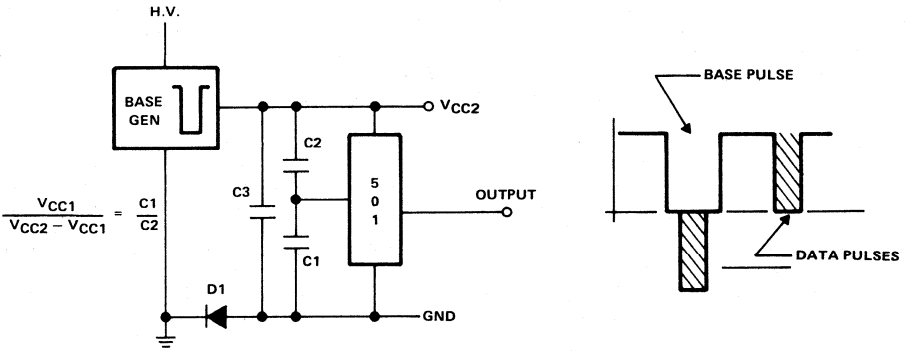


Figure 18. Floating SN75501A Fixed Bias

small (typically 200 mA) when drawn from the high-voltage supply (100 V), it represents a significant power dissipation.

$$200\ mA \times 100\ V \times 1\ \mu s = 20\ \mu J$$

The average power consumed depends then on the operating frequency of the system.

$$\text{at 50 kHz: } 20\ \mu J \times 50\ kHz = 1\ W$$

The SN75500A is designed such that the data registration and retention circuitry are powered from the V_{CC1} supply (12 V). The high-voltage supply, V_{CC2} is required only to provide pull-up of the SN75500A outputs when a positive output pulse is desired. It is most beneficial therefore to blank the V_{CC2} input except for the period of time the outputs of the SN75500A are switched high (strobed). Utilization of this feature (strobing the high voltage) allows lower power dissipation and improved performance with the SN75500A. Figure 20 shows a typical circuit which provides for strobed application of the V_{CC2} supply.

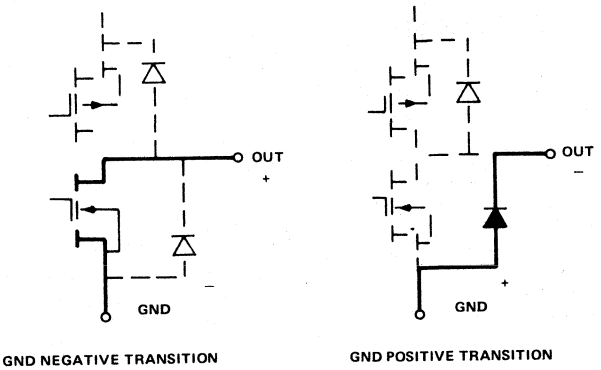


Figure 19. Floating SN75500A Current Paths

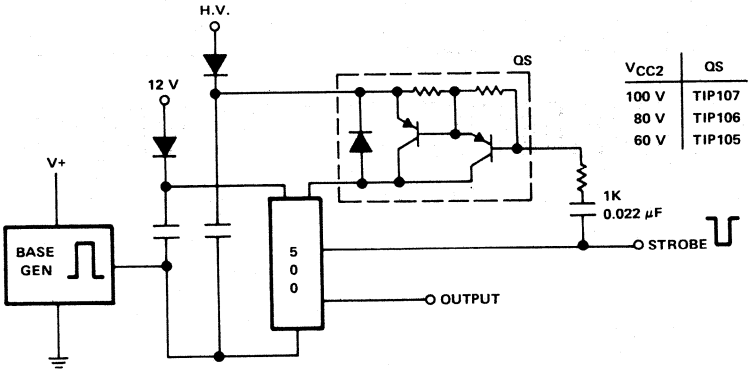


Figure 20. Floating SN75500 with Pulsed V_{CC2}

DATA COUPLING CONSIDERATIONS

If operated ground-based, all inputs are CMOS compatible ($V_{TH} \approx 5$ V). If, however, either driver is floated on a base, signal entry of data into that device must be given due consideration.

One simple approach not necessarily cost effective, but simple, employs the use of coupling transformers on all data lines: clock, serial data in, strobe, sustain, select. In this configuration, data can be entered into the device regardless of the state of the base signal. This provides the maximum utilization of the drivers by minimizing the time required to shift data into the drivers' storage registers. Another approach requires gating of the data but creates a totally solid-state interface. In this approach, data is gated into the drivers when they reside at ground. Figure 21 shows a typical application in which a base pulse is employed and illustrates the timing of the gated clock which registers the data in the respective driver. Considering 4 MHz is the maximum data rate, 8 microseconds is required to fill the 32-bit shift register of the SN75501. The frequency and duty cycle of the base pulse then decide whether the data can be entered in a single cycle. The limiting factor in most applications is the speed of the source from which the data is received.

Figure 22 shows a circuit for use with positive base signals. When the base pulse is at ground, the input signal operates as a pull-up to the input of the CMOS buffer through the blocking diode. As the ground bias of the buffer circuit rises with its associated plasma driver, the diode becomes reverse biased and the resistive termination of the input maintains a logic zero at its input. With this circuit, transitions in the floating bias applied to the buffer gate are not detectable at its output, providing the input signal is low.

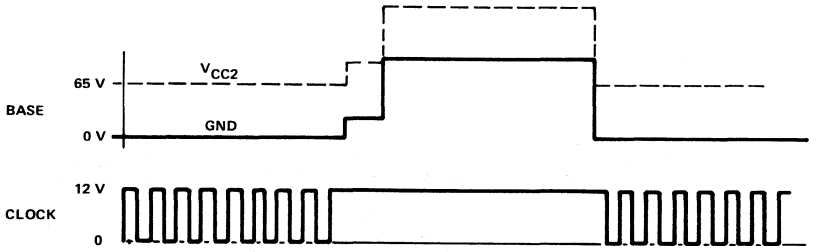


Figure 21. Gated Clock for Floating Applications

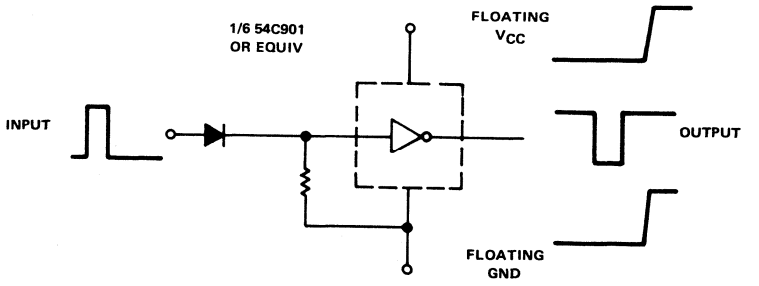


Figure 22. Positive Base Signal Data Buffer Circuit

Figure 23 shows a similar interface circuit for use with negative base signals. Note the reversal of the blocking diode. This circuit uses a normally high (logic 1) input signal. While ground based, the buffer gate will respond to logic zero transitions at its input. As the ground and V_{CC} inputs of the buffer circuit go below ground, the blocking diode becomes reverse biased and the terminating resistor establishes a logic 1 (high) input on the gate input. Thus providing the input is at a logic 1, transitions in the ground and V_{CC} bias inputs concurrent with the respective plasma driver will not affect the output of the buffer. The use of the inverting or noninverting buffer gate is determined primarily on the preferred status of the output signal during the period of time the driver is floating. Both circuits of Figures 22 and 23 create normally high (logic 1) signals. This is the preferred state of the positive edge triggered clock circuits of the SN75500A and SN75501A plasma drivers.

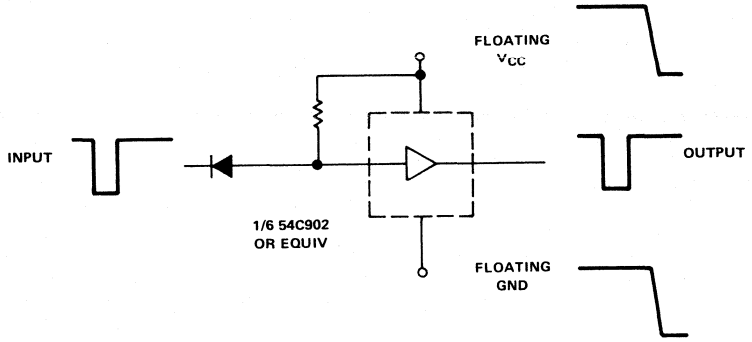


Figure 23. Negative Base Signal Data Buffer Circuit

BIDFET Process High Voltage IC Technology

BIDFET is a rugged, low-cost wafer processing technology which merges precision control, self-isolated CMOS logic and high-voltage interface circuitry on a common monolithic substrate, manufactured using standard junction isolation techniques. Many multi-technology processes have been developed but BIDFET is the only merged process which attacks the high voltage limitations of conventional integrated circuits while retaining their LSI logic capabilities. BIDFET devices have been produced with working voltages to 250V and breakdown voltages exceeding 300V. This is achieved by replacing the conventional bipolar output stage with a Double-Diffused MOS (DMOS) transistor structure.

Operation of a bipolar device such as a switch, within the Reverse Bias Safe Operating Area (RBSOA), requires several considerations.

Figure 1 shows the typical load/line characteristics of a switch operated within the devices RBSOA and $V_{CES(SUS)}$ ratings. As shown, the load/line penetrates the RBSOA. This condition is destructive. Thus, reliable operation is limited to the $V_{BR(CEO)}$ rating of the switch, which is limited by either the vertical (X) or lateral (Y) characteristics of the structure, whichever is the lesser.
For a structure shown in Figure 2, the expressions for these characteristics are:

$$V_{BR(CEO)}[X] = \sqrt[-4]{B_X} \int_{X_B}^{X_{epi}} E_x dx$$

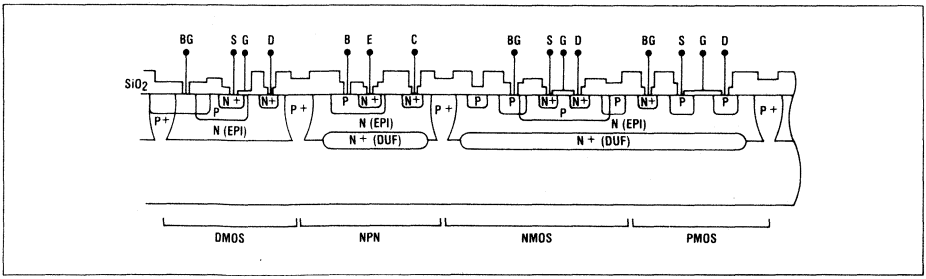
$$V_{BR(CEO)}[Y] = \sqrt[-4]{B_y} \int_{0}^{Y_c} E_y dy$$

With common topologies used in conventional integrated circuits, breakdown voltages [$V_{BR(CEO)}$] are limited by the thickness of the epitaxial layer (X_{EPI}). Practical limitations on the thickness of conventional junction isolated integrated circuits limit their $V_{BR(CEO)}$ to 70 volts.

The DMOS structure, on the other hand, is a surface (lateral) device whose breakdown characteristic is limited only by bulk junction avalanching and horizontal topology (channel length). Breakdown ratings are governed by doping levels and surface area, which is an economic consideration, instead of a physical limitation. Unlike NPN transistors, DMOS can operate safely to its breakdown voltage limit without risk of destructive secondary breakdown or sacrifice of reliability. Figure 3 shows the breakdown characteristics of the two structures.

Characteristic waveforms (Figure 4) show the virtual independence of the output current to the output voltage of a DMOS structure. The early voltage, as well as the stored charge characteristics of the DMOS structure, is superior to that of the bipolar transistor in switching applications.

With the variety of structures offered by the BIDFET process, design engineers can idealize high voltage circuits by partitioning their circuits and using the optimum technologies for the various sections. The bipolar structure offers durability and is very forgiving of input conditions. CMOS allows increased circuit complexity while requiring minimal power consumption and bar area. The DMOS structure's benefits have been presented herein. The result is a high-voltage interface circuit which is capable of performing data registration, manipulation or decoding functions to reduce the requirements on system electronics.



BIDFET Cell Cross-Section

BIDFET Process High Voltage IC Technology

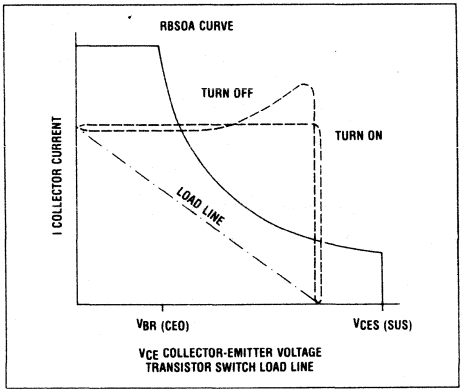


Figure 1

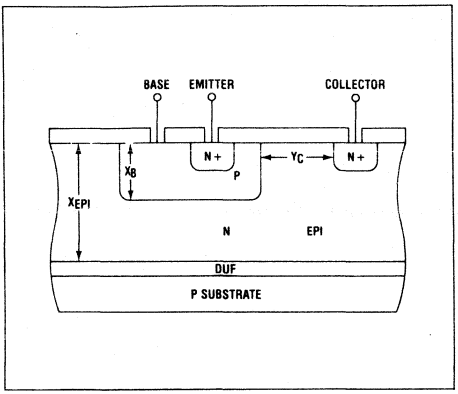


Figure 2 NPN Transistor

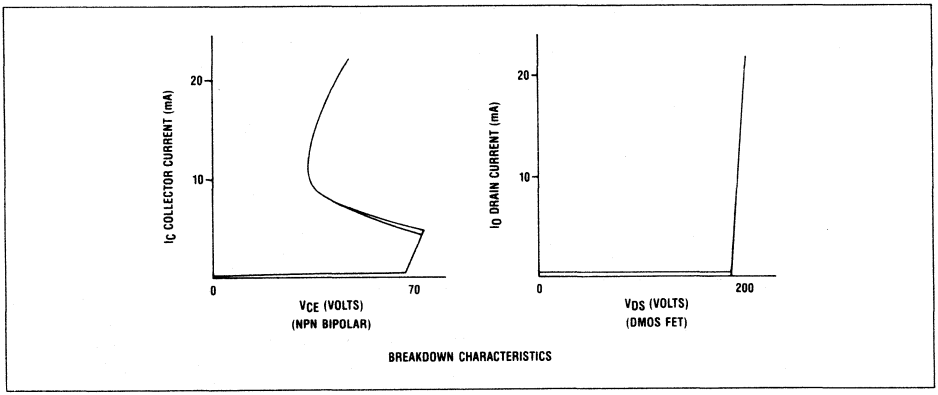


Figure 3 Breakdown Characteristics

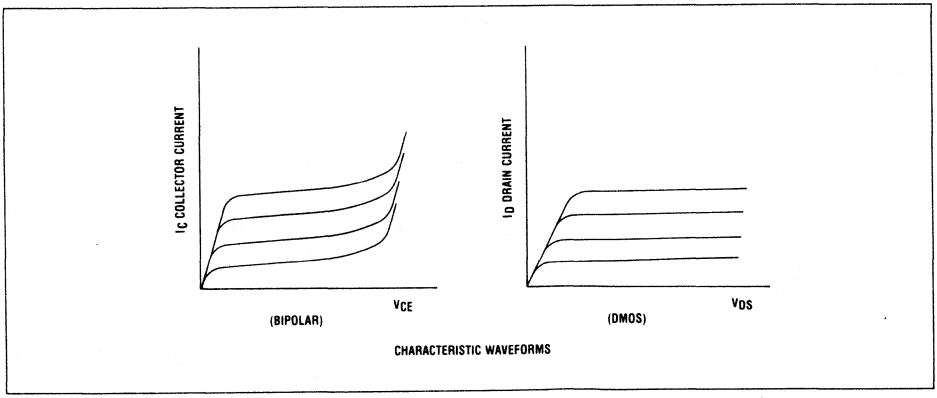


Figure 4 Characteristic Waveforms

DISPLAY DRIVERS

Commercial Temperature Range

Display Type	Description	Input Compatibility	Power Supplies	Drivers Per Package	Device Type	Package Type	Additional Features
AC Plasma Displays	Axis Drivers	CMOS	VCC1 = 12V, VCC2 variable from 40V to 90V	4	SN75426B	J,N	• Independent addressing of each gate for serial and and parallel applications. • High input impedance (typically 1 megohm) • 30mA clamp diodes on output. • Switches 70V in 1.2μs. • AND driver (SN75426); NAND driver (SN75427)
					SN75427B	J,N	
		CMOS	VCC1 = 12V, VCC2 variable From VCC1 to 100V	32	SN75500A	N	• High-speed serially shifted data input (4MHz max). • Fast output transions (less than 150ns). • 25mA output current capability. •Output short-circuit capability. • Static shift registers can retain data on all outputs of SN75501 and SN75503A indefinitely. • X-axis driver – SN75500A and SN75502A • Y-axis driver – SN75501A and SN75503A perform Y-axis sustaining function
		TTL			SN75502A	N	
		CMOS			SN75501A	N	
		TTL			SN75503A	N	
LED Displays	Segment Drivers	MOS	10V	§	SN75491	N	• 50mA source/sink capability.
			20V	4	SN75491A	N	
			Variable from 3.2V to 8.8V	4	SN75493	N	• 50mA regulated source capability. • Display blanking provisions.
	Digit Drivers	MOS	10V	6	SN75492	N	• 250mA sink capability.
			20V	6	SN75492A	N	
			Variable from 3.2V to 8.8V	6	SN75494	N	• 250mA sink capability. • Display blanking provisions.
		TTL	10V	6	SN75496	N	• 250mA sink capability.
			20V	6	SN75496A	N	
		MOS TTL	Variable from 2.7V to 6.6V	7	SN75497	N	• 100mA sink capability. • Input threshold...2.7V max. • Low voltage saturating outputs (0.4V maximum)
		MOS MTL	Variable from 2.7V to 6.6V	9	SN7549B	N	• 100mA sink capability • Input threshold...2.7V max
Gas Discharge Displays	High-voltage BCD-to-seven segment Decoder Cathode Drivers	TTL	5V	7	SN75480	N	• Outputs regulated to ensure constant brightness. • Blanking and ripple-blanking provisions. • High off-state breakdown voltage (120V typical). • Designed for seven segment displays such as Beckman and Panaplex II*
		CMOS	Variable from 5V to 15V	7½	SN75580	N	Same features as the SN75480 plus: • Decimal point provided. • Latches to hold BCD information. • Lower supply power requirments. • Higher output voltage breakdown capability.
		TTL	Variable from 4.75V to 15V	7½	SN75584A	N	
	Anode Driver	MOS	VEE = −55V VBB = −18V	6	SN75481	N	• 13mA output capability. • Designed for time-multiplied displays.
Thermal Print Displays	Thermal Printhead Drivers	TTL, CMOS	±5V	6	SN75490	J,N	• Common strobe • 30mA source, 50mA sink capability
		MOS	5V	7	SN75270	J,N	• Single ended, noninverting operation.
Vacuum Fluorescent Displays	Drivers	TTL CMOS	VCC1 = 12V VCC2 = 60V	12	SN75513	N	• 12 output drivers for dot-matrix or segmented displays. • 60V, 25mA outputs. • Serial input • SN75512 has latched outputs for continuous display.
				12	SN75512	N	
				32	SN75518	N	60V, 24mA outputs

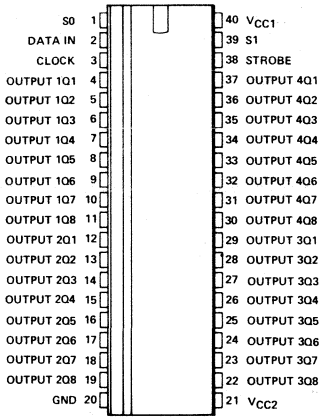
* Trademark of the Burroughs Corporation.

TYPES SN75500A, SN75502A AC PLASMA DISPLAY X-AXIS DRIVERS

BULLETIN NO. DL-S 12622, APRIL 1980

- Each Device Drives 32 Axis Lines
- High-Speed Serially Shifted Data Input Operation (4 MHz max)
- 100-V Output Voltage Swing Capability
- 20-mA Output Current Operation
- Low-Power Nonswitching Operation
- Fast Output Transitions
- Totem Pole Outputs
- Sink and Source Clamp Diodes
- SN75500A Has CMOS-Compatible Inputs
- SN75502A Has TTL-Compatible Inputs
- Selects 1 of 8 Lines Within 1 of 4 Groups
- Shift Register Can Retain Data on All Outputs Indefinitely While Clock is High

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

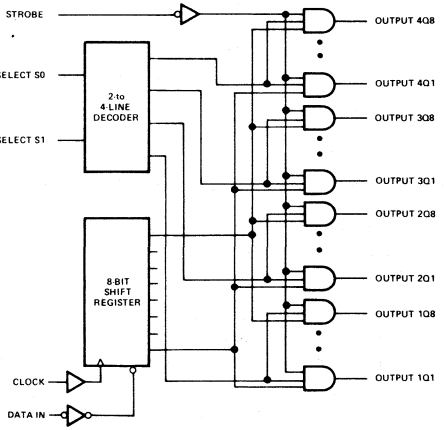


description

The SN75500A and SN75502A are monolithic BIDFET integrated circuits (bipolar, double-diffused MOS, n-channel MOS, and p-channel MOS transistors on the same chip†) designed to perform the select operation along the X-axis of a plasma display. The SN75500A is designed with CMOS-compatible inputs while the SN75502A is designed to be driven by TTL circuitry.

These devices each have an 8-bit shift register and a 2-to-4-line decoder, which steers the 8-bit data string to one of four groups of eight outputs. The shift register has indefinite latch capability when the clock input is held high. The decoder is controlled by inputs S0 and S1. The outputs are activated by the strobe input. When the strobe input is driven low, the selected 8-bit output group reflects the inverted data input string while the other twenty-four outputs remain low. With a capacitive load, this requires minimal power for driving the output.

functional block diagram



The device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open circuited. The nominal input threshold is 5 volts for the SN75500A and 1.5 volts for the SN75502A. The device outputs are totem-pole structures formed by double-diffused MOS (DMOS) transistors with clamp diodes to both ground and V_{CC2}.

†Patent pending

FUNCTION TABLE

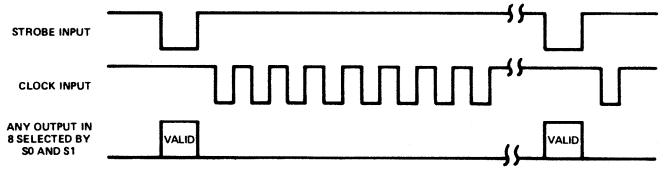
FUNCTION	INPUTS					OUTPUTS					
	DATA	CLOCK	S1	S0	STROBE	SHIFT REGISTERS R1	R2	R3 . . . R8	1Q1 . . . 1Q8	2Q1 . . . 2Q8	3Q1 . . . 3Q8	4Q1 . . . 4Q8
LOAD	H	↑	X	X	H	L	$R1_n$	$R2_n$ . . . $R7_n$	L . . . L	L . . . L	L . . . L	L . . . L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ . . . $R7_n$	L . . . L	L . . . L	L . . . L	L . . . L
STROBE	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	L . . . L	L . . . L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	R1 . . . R8	L . . . L	L . . . L	L . . . L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	R1 . . . R8	L . . . L	L . . . L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	R1 . . . R8	L . . . L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	L . . . L	R1 . . . R8

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition

R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.

$R1_n$ . . . $R8_n$ = levels at internal outputs of shift registers one through eight, respectively, before the most recent low-level pulse at the clock input.

typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 1056 mW at 70°C at the rate of 13.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	V_{CC1}		100	V
Peak high-level output current			−20	mA
Peak low-level output current			20	mA
High-level output clamp current			20	mA
Low-level output clamp current			−20	mA
Input data rate	0		4	MHz
Width of high clock pulse, t_{wH}	125			ns
Width of low clock pulse, t_{wL}	125		600	ns
Data setup time before low-to-high transition of clock, t_{su}	125			ns
Data hold time after low-to-high transition of clock, t_h	0			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN75500A			SN75502A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage			7			2			V
V_{IL}	Low-level input voltage					3			0.8	V
V_{IK}	Input clamp voltage	V_{CC1} = 12 V, I_I = −12 mA			−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	95	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		92	94.5		
			I_{OH} = −15 mA	91	93.5		91	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 100 V	I_O = 20 mA		101	102.5		101	102.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	$V_I = V_{IH}$ min		−0.1	40		0.1	40	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	$V_I = V_{IL}$ max		−20	−150		−20	−150	μA
I_{CC1}	Supply current	V_{CC1} = 13,2 V	$V_I = V_{IH}$ min		1	2		1	2	mA
			$V_I = V_{IL}$ max		8	12		8	12	mA
I_{CC2}	Supply current	V_{CC2} = 100 V	Eight outputs high		1	3		1	3	mA
			All outputs low		1	2		1	2	mA

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 65 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION

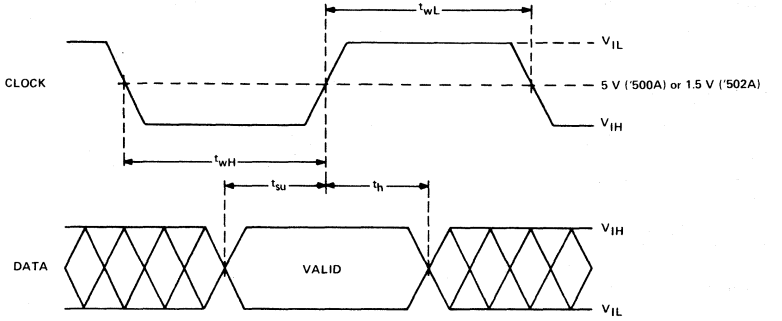


FIGURE 1–DATA INPUT TIMING

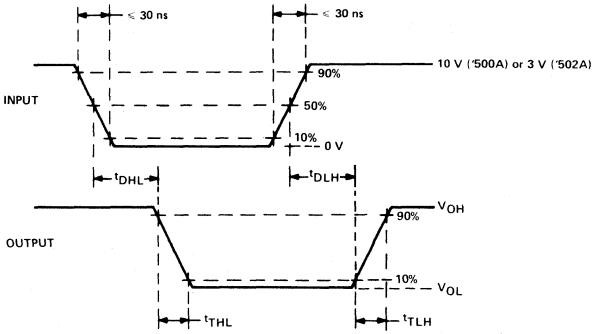
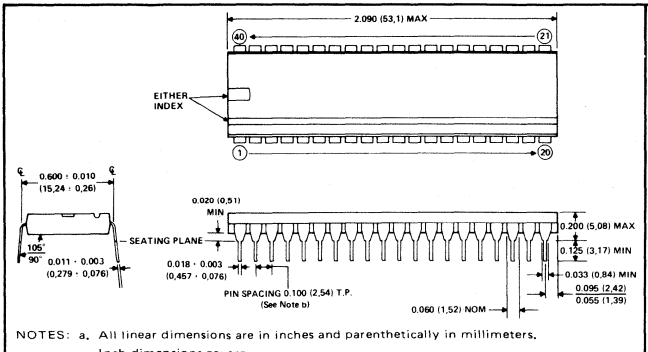
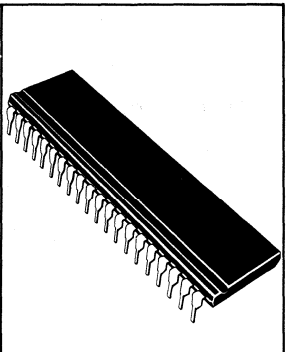


FIGURE 2–OUTPUT SWITCHING TIMES

MECHANICAL DATA

40-pin N plastic dual-in-line package





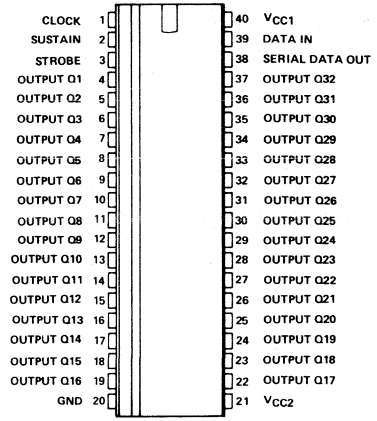
NOTES: a. All linear dimensions are in inches and parenthetically in millimeters.
Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TYPES SN75501A, SN75503A AC PLASMA DISPLAY Y-AXIS DRIVERS

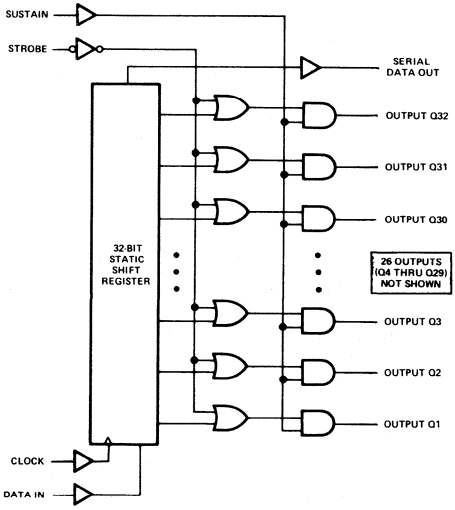
BULLETIN NO. DL-S 12621, APRIL 1980

- Each Device Drives 32 Axis Lines
- High-Speed Serially Shifted Data Input Operation (4 MHz Max)
- 100-V Output Voltage Swing Capability
- 20-mA Output Current Operation
- Low-Power Nonswitching Operation
- Fast Output Transitions
- Totem-Pole Outputs
- Sink and Source Clamp Diodes
- SN75501A Has CMOS-Compatible Inputs
- SN75503A Has TTL-Compatible Inputs
- Performs Y-Axis Sustaining Function
- Static Shift Register Can Retain Data on all Outputs Indefinitely

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram



description

The SN75501A and SN75503A are monolithic BIDFET integrated circuits (bipolar, double-diffused MOS, n-channel MOS, and p-channel MOS transistors on the same chip†) designed to perform the select operation and the sustain function along the Y-axis of a plasma display. The SN75501A is designed with CMOS-compatible inputs while the SN75503A is designed to be driven by TTL circuitry.

These devices each have a 32-bit shift register with indefinite latch capability when the clock input is either high or low. Information at the data input meeting the setup time requirements is transferred into the shift register on the positive-going edge of the clock signal. Each shift register output drives its respective Q output through two gates controlled by the strobe and sustain inputs, respectively. The strobe input controls the outputs for writing and erase functions, while the sustain input controls the output for system sustaining along the Y-axis. The serial-data output can be used to cascade shift registers.

The device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 5 volts for the SN75501A and 1.5 volts for the SN75503A. The device outputs are totem-pole structures formed by double-diffused MOS (DMOS) transistors with clamp diodes to both ground and V_{CC2}.

† Patent pending

FUNCTION TABLE

FUNCTION	INPUTS				OUTPUTS						
	DATA IN	CLOCK	STROBE	SUSTAIN	SHIFT REGISTERS R1	R2	R3 . . . R32	SERIAL DATA	Q1	Q2	Q3 . . . Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . HI
	L	↑	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . HI
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	H	H	H . . . HI
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	R1	R2	R3 . . . R32
SUSTAIN	X	X	X†	L	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	L	L	L . . . L

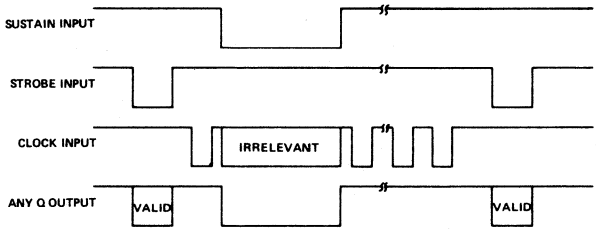
H = high level, L = low level, X = irrelevant, ↑ = low-to-high level transition.

R1 . . . R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.

$R1_n$ . . . $R32_n$ = levels at internal outputs of shift registers one through thirty-two, respectively, before the most recent low-level pulse at the clock input.

†To minimize delay time for the next output signals, it is recommended that Strobe remain high while Sustain is low. Delay time from Strobe to the Q outputs is typically longer than from Sustain.

typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 1056 mW at 70°C at the rate of 13.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	V_{CC1}		100	V
Peak high-level output current			−20	mA
Peak low-level output current			20	mA
High-level output clamp current			20	mA
Low-level output clamp current			−20	mA
Input data rate	0		4	MHz
Width of high clock pulse, t_{wH}	125			ns
Width of low clock pulse, t_{wL}	125			ns
Data setup time before low-to-high transition of clock, t_{su}	125			ns
Data hold time after low-to-high transition of clock, t_h	0			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN75501A			SN75503A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH} High-level input voltage				7			2			V
V_{IL} Low-level input voltage						3			0.8	V
V_{IK} Input clamp voltage		V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5		−1	−1.5	V
V_{OH} High-level output voltage	Outputs 1 through 32	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	95	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		92	94.5		
			I_{OH} = −15 mA	91	93.5		91	93.5		
	Serial data	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		9	10		
V_{OL} Low-level output voltage	Outputs 1 through 32	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5	
	Serial data	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1		0.1	1	
V_{OK} Output clamp voltage		V_{CC2} = 100 V	I_O = 20 mA		101	102.5		101	102.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH} High-level input current		V_{CC1} = 13.2 V,	$V_I = V_{IH}$ min		0.1	40		0.1	40	μA
I_{IL} Low-level input current		V_{CC1} = 13.2 V,	$V_I = V_{IL}$ max		−20	−150		−20	−150	μA
I_{CC1} Supply current		V_{CC1} = 13.2 V	$V_I = V_{IH}$ min		0.5	2		0.5	2	mA
			$V_I = V_{IL}$ max		6	12		6	12	mA
I_{CC2} Supply current		V_{CC2} = 100 V	All outputs high		1	3		1	3	mA
			All outputs low		1	3		1	3	mA

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 65 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{DHL}	Delay time, high-to-low-level output from sustain input			250	ns
t_{DLH}	Delay time, low-to-high-level output from sustain input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION

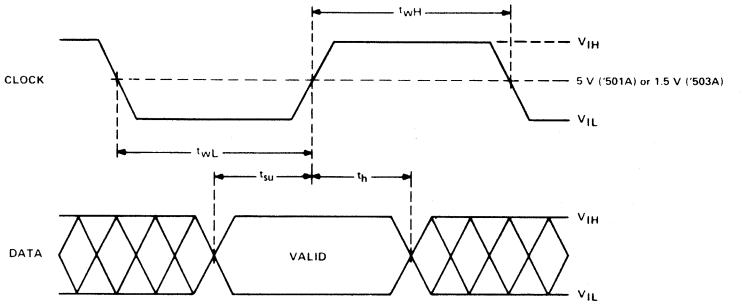


FIGURE 1–DATA INPUT TIMING

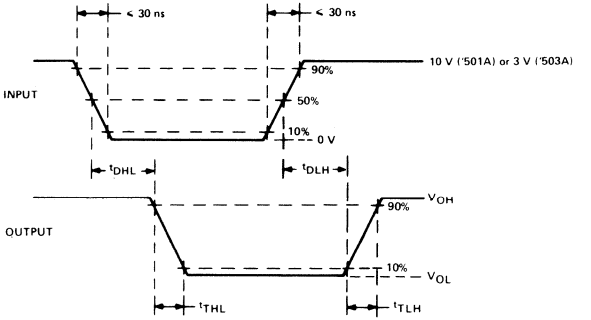
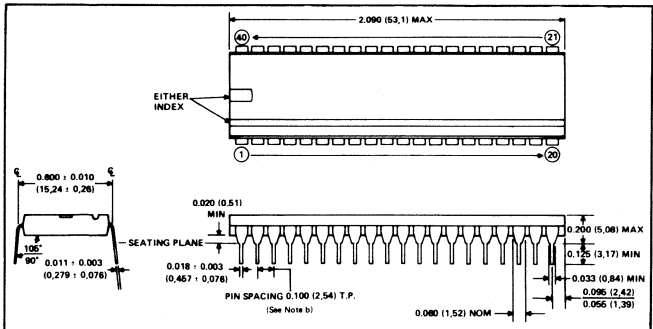
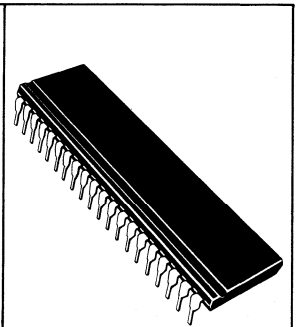


FIGURE 2–OUTPUT SWITCHING TIMES

MECHANICAL DATA

40-pin N plastic dual-in-line package





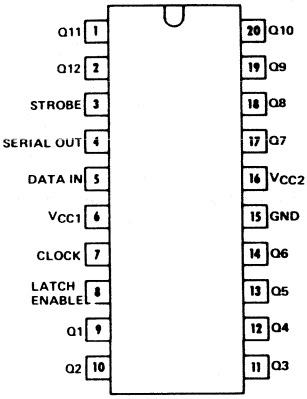
NOTES: a. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TYPE SN75512A
VACUUM FLUORESCENT DISPLAY DRIVER

D2654, OCTOBER 1981

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Inputs
- Latches on All Driver Outputs.

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

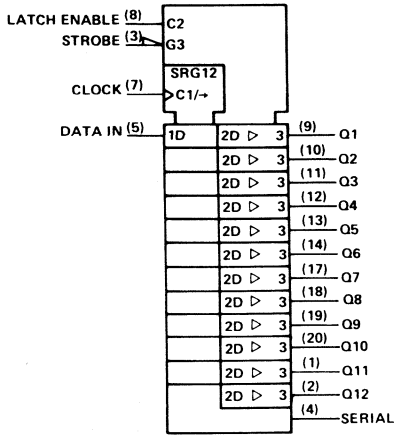
The SN75512A is a monolithic BIDFET integrated circuit (bipolar, double-diffused, n-channel MOS and p-channel MOS transistors on same chip†) designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 volts. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

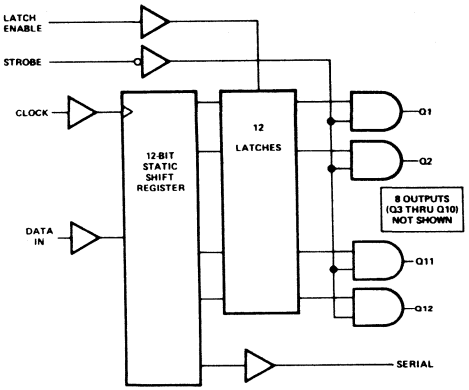
The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock. When high, the latch enable input transfers the shift register contents to the outputs of the 12 latches. The active-low strobe input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the latch enable or strobe inputs.

The SN75512A is characterized for operation from 0°C to 70°C. .

logic symbol‡



functional block diagram



†Patent Pending

‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

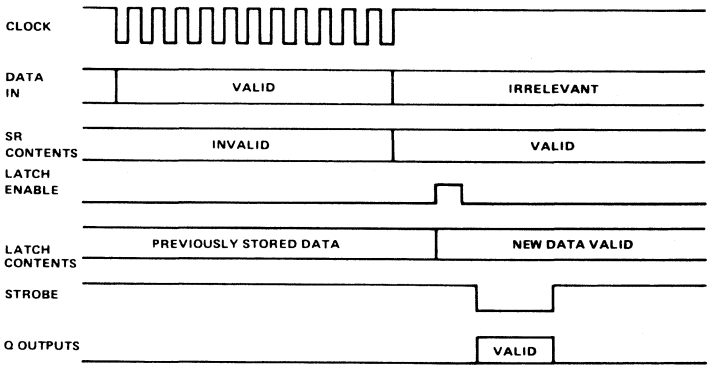
TYPE SN75512A
VACUUM FLUORESCENT DISPLAY DRIVER

FUNCTION TABLE

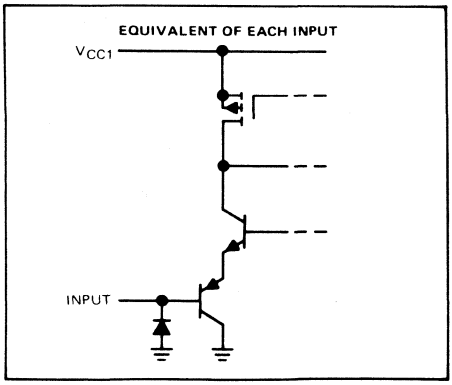
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R12*	Determined by Strobe
	Not↑	X	X	No change	Determined by Latch Enable§	R12	Determined by Strobe
LATCH	X	L	X	As determined above	Stored data	R12	Determined by Strobe
	X	H	X	As determined above	New data	R12	Determined by Storbe
STROBE	X	X	H	As determined above	Determined by Latch Enable§	R12	All L
	X	X	L	As determined above	Determined by Latch Enable§	R12	LC1 thru LC12, respectively

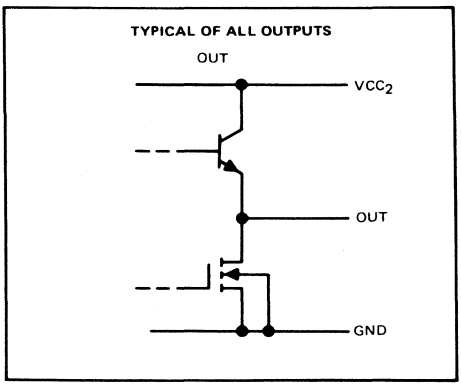
H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition.
§ New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.
* R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 60 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 70°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	5		15	V
Supply voltage, V_{CC2}	0		60	V
Peak high-level output current			−25	mA
Peak low-level output current			200	μA
Input data rate	0		1	MHz
Width of high clock pulse, t_{wH} (see Figure 1)	500			ns
Width of low clock pulse, t_{wL} (see Figure 1)	500			ns
Data setup time before low-to-high transition of clock, t_{su} (see Figure 1)	250			ns
Data hold time after low-to-high transition of clock, t_h (see Figure 1)	250			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP¶	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
V_{IK}	Input clamp voltage		V_{CC1} = 10 V,	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 10 V,	V_{CC2} = 60 V,	I_O = −25 mA	55	57.5		V
		Serial data	V_{CC1} = 10 V,	I_{OH} = −200 μA		9	9.3		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 10 V,	I_{OL} = 1 mA			1	5	V
		Serial data	V_{CC1} = 10 V,	I_{OL} = 200 μA			0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 15 V			0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0 V				−150	μA
I_{CC1}	Supply current		V_{CC1} = 15 V,		V_I = 15 V			800	μA
					V_I = 0 V		10	12	mA
I_{CC2}	Supply current		V_{CC1} = 15 V, V_{CC2} = 60 V		All outputs high		5	8	mA
					Strobe at 2 V		100	500	μA

¶ Typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		500	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			500	ns
t_{THL}	Transition time, high-to-low-level output			300	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION

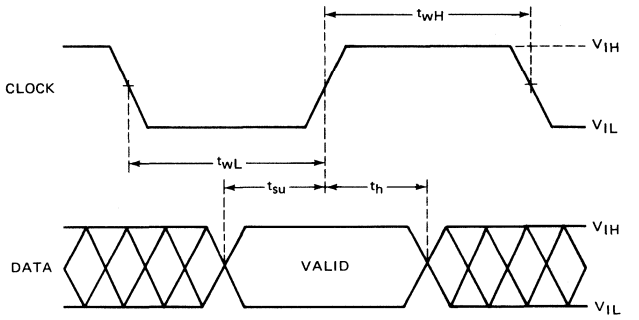


FIGURE 1 – INPUT TIMING VOLTAGE WAVEFORMS

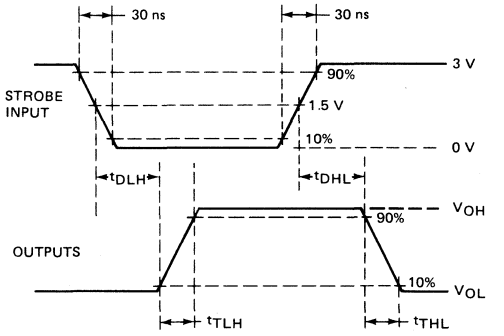
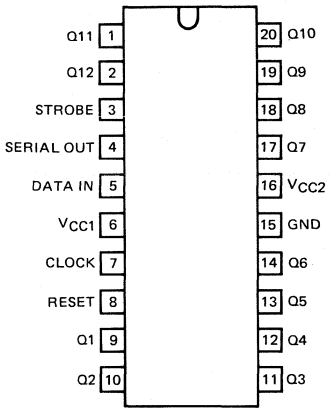


FIGURE 2 – SWITCHING-TIME VOLTAGE WAVEFORMS

TYPE SN75513A
VACUUM FLUORESCENT DISPLAY DRIVER

- **Each Device Drives 12 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **TTL-Compatible Inputs**
- **Reset Input**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

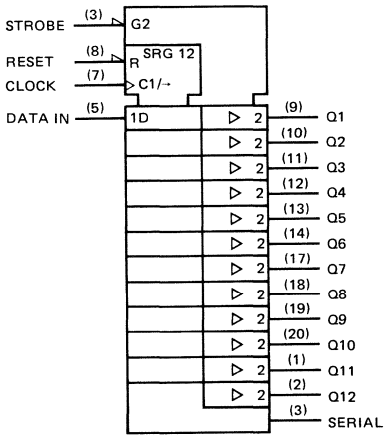
The SN75513A is a monolithic BIDFET integrated circuit (bipolar, double-diffused, n-channel MOS and p-channel MOS transistors on same chip†) designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 volts. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

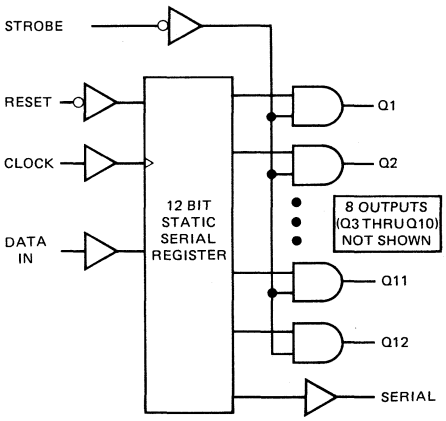
The device consists of a 12-bit shift register and 12 output AND gates. Data is entered into the shift register on the low-to-high transition of the clock. The active-low strobe input enables all Q outputs. The reset input sets the shift register contents to all lows. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the strobe input.

The SN75513A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram



† Patent Pending
‡ This symbol is in accordance with IEEE Std 91/ANSI Y32 14 and current discussions in IEC and IEEE

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

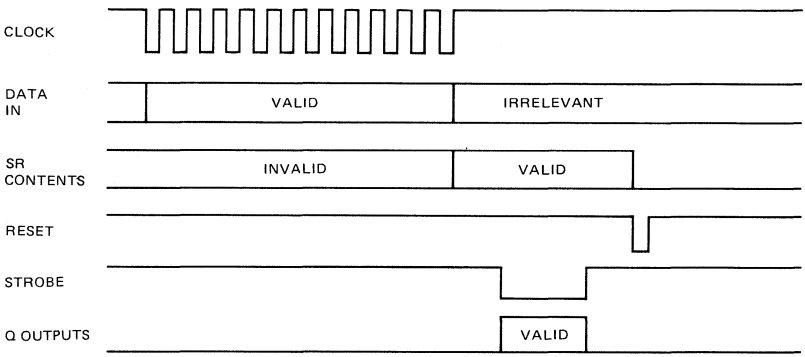
TYPE SN75513A
VACUUM FLUORESCENT DISPLAY DRIVER

FUNCTION TABLE

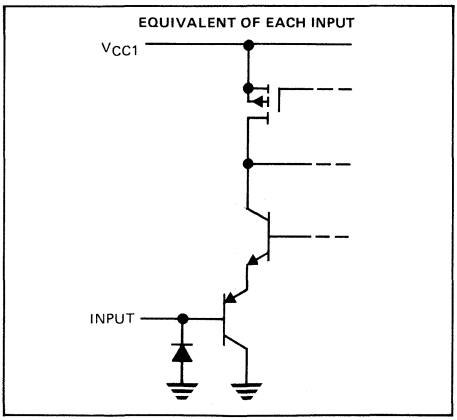
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS		OUTPUTS
	RESET	CLOCK	STROBE	R1 THRU R12	SERIAL	Q1 THRU Q12
LOAD	H	↑	X	Load and shift*	R12*	Determined by Strobe
STROBE	H	No↑	H	No change	R12	All L
	H	No↑	L	No change	R12	R1 thru R12, respectively
RESET	L	H	X	All L	L	All L

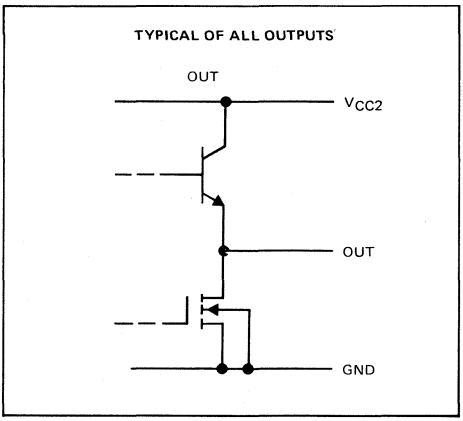
H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
*R12 and Serial output take on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 60 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 70°C free-air temperature . . . . . 840 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	5		15	V
Supply voltage, V_{CC2}	0		60	V
Peak high-level output current			25	mA
Peak low-level output current			200	μA
Input data rate	0		1	MHz
Width of high clock pulse, t_{wH} (see Figure 1)	500			ns
Width of low clock pulse, t_{wL} (see Figure 1)	500			ns
Data set up time before low-to-high transition of clock, t_{su} (see Figure 1)	250			ns
Data hold time after low-to-high transition of clock, t_h (see Figure 1)	250			ns
Operating free-air temperature, T_A	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC1} = 10 V, I_I = 12 mA				1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 10 V, V_{CC2} = 60 V, I_O = 25 mA		55	57.5		V
		Serial data	V_{CC1} = 10 V, I_{OH} = 200 μA		9	9.3		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 10 V, I_{QL} = 1 mA			.1	5	V
		Serial data	V_{CC1} = 10 V, I_{QL} = 200 μA			0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V			0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V			−	150	μA
I_{CC1}	Supply current		V_{CC1} = 15 V,	V_I = 15 V			800	μA
				V_I = 0 V		10	12	mA
I_{CC2}	Supply current		V_{CC1} = 15 V, V_{CC2} = 60 V	All outputs high		12	14	mA
				Strobe at 2 V		100	500	μA

Typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		300	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			300	ns
t_{THL}	Transition time, high-to-low-level output			500	ns
t_{TLH}	Transition time, low-to-high-level output			500	ns

PARAMETER MEASUREMENT INFORMATION

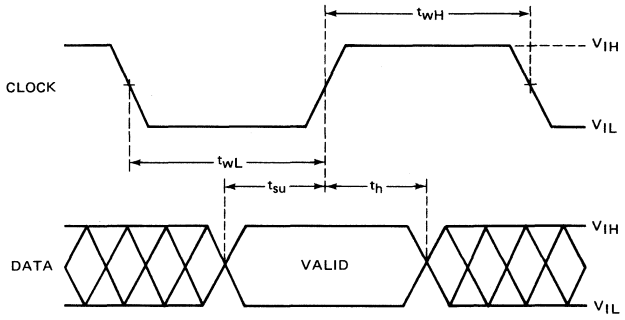


FIGURE 1 – INPUT TIMING VOLTAGE WAVEFORMS

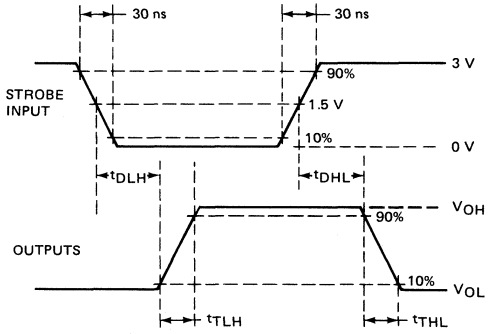
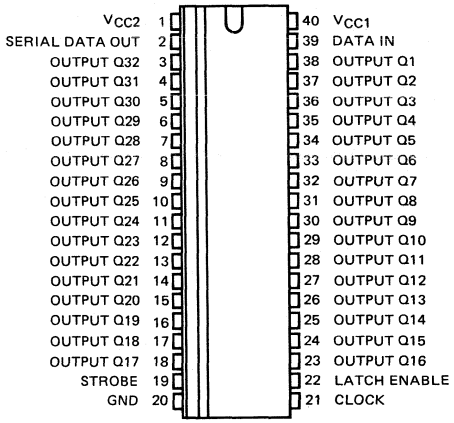


FIGURE 2 – SWITCHING-TIME VOLTAGE WAVEFORMS

TYPE SN75518
VACUUM FLUORESCENT DISPLAY DRIVER

- Each Device Drives 32 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- Totem Pole Outputs
- Latches on All Driver Outputs.

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

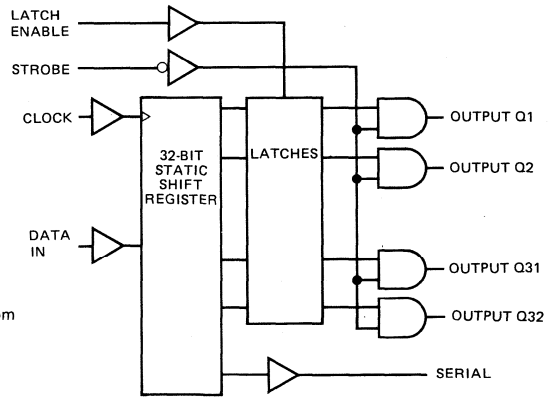


description

The SN75518 is a monolithic BIDFET integrated circuit (bipolar, double-diffused, n-channel MOS and p-channel MOS transitors on same chip†) designed to drive a dot matrix or segmented vacuum fluorescent display.

The device consists of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transistion of the clock. When high, the latch enable input transfers the shift register contents to the outputs of the 32 latches. The active-low strobe input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the latch enable or strobe inputs.

functional block diagram



The SN75518 is characterized for operation from 0°C to 70°C.

TENTATIVE DATA SHEET

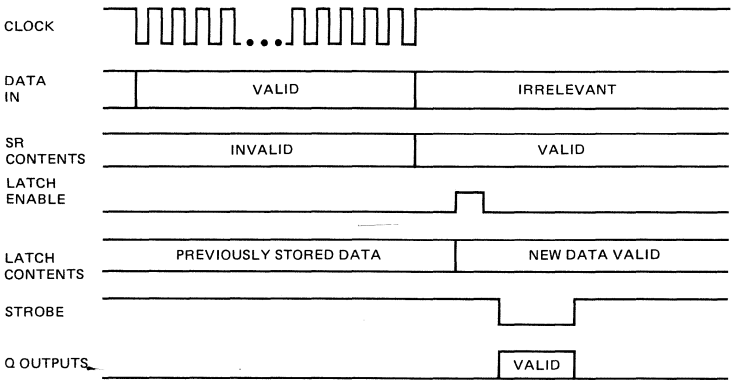
This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

FUNCTION TABLE

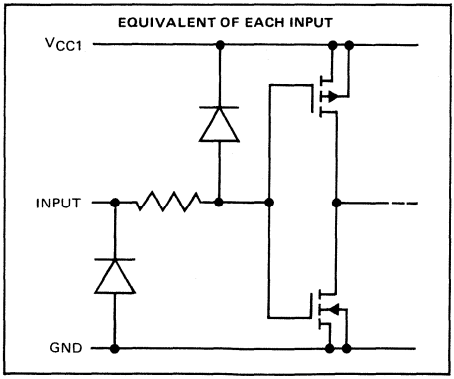
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable §	R32*	Determined by Strobe
	No↑	X	X	No change	Determined by Latch Enable §	R32	Determined by Strobe
LATCH	X	L	X	As determined above	Stored data	R32	Determined by Strobe
	X	H	X	As determined above	New data	R32	Determined by Strobe
STROBE	X	X	H	As determined above	Determined by Latch Enable §	R32	All L
	X	X	L	As determined above	Determined by Latch Enable §	R32	LC1 thru LC32 respectively

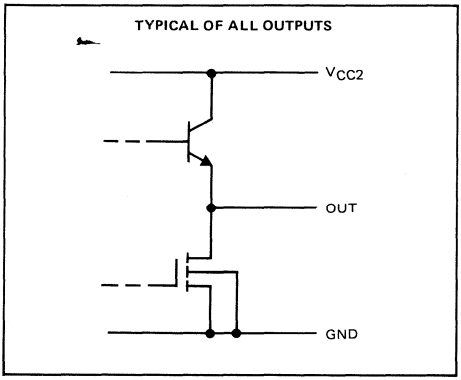
H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition.
§New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 60 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 70°C free-air temperature . . . . . 850 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.5		12	V
Supply voltage, V_{CC2}	0		60	V
Peak high-level output current			−25	mA
Peak low-level output current			2	mA
Input data rate (V_{CC1} = 4.5)	0		1	MHz
Input data rate (V_{CC1} = 10V)	0		5	MHz
Width of high clock pulse, t_{wH} (see Figure 1) (VCC1 = 10 V)	100			ns
Width of low clock pulse, t_{wL} (see Figure 1) (V_{CC1} = 10 V)	100			ns
Width of high clock pulse, t_{wH} (see Figure 1) (V_{CC1} = 4.5 V)	500			ns
Width of low clock pulse, t_{wL} (see Figure 1) (V_{CC1} = 4.5 V)	500			ns
Data setup time before low-to-high transition of clock, t_{su} (see Figure 1) (V_{CC1} = 4.5 V)	150			ns
Data hold time after low-to-high transition of clock, t_h (see Figure 1) (V_{CC1} = 4.5 V)		150		ns
Data setup time before low-to-high transition of clock, t_{su} (see Figure 1) (V_{CC1} = 10V)	75			ns
Data hold time after low-to-high transition of clock, t_h (see Figure 1) (V_{CC1} = 10 V)	75			ns
Operating free-air temperature, T_A	0		70	C

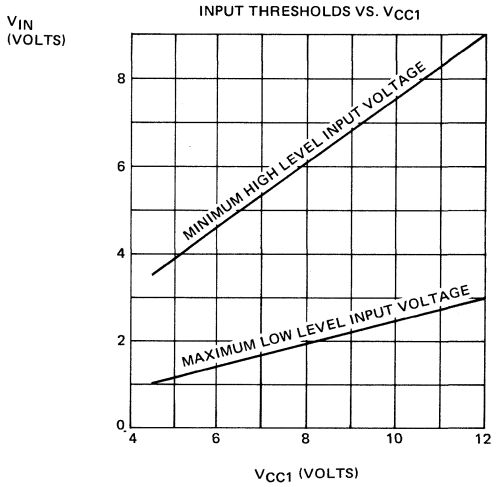
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

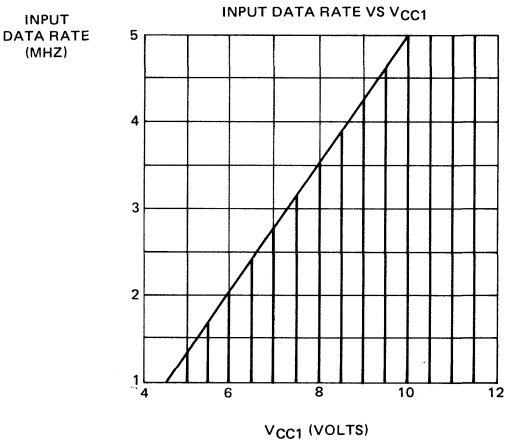
PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IH}	High-level input voltage		V_{CC1} = 4.5 V			3.5 V		V
V_{IL}	Low-level input voltage		V_{CC1} = 4.5 V				1.0	V
V_{IH}	High-level input voltage		V_{CC1} = 12V			9.0		V
V_{IL}	Low-level input voltage		V_{CC1} = 12V				3.0	V
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 5 V,	V_{CC2} = 60 V,	I_O = −25 mA	58	59	V
		Serial data	V_{CC1} = 5 V,	I_{OH} = −20 μA		4.5	5.0	
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 5 V,	I_{OL} = 1 mA			1.0	V
		Serial data	V_{CC1} = 5 V,	I_{OL} = 20 μA			0.8	
I_{IH}	High-level input current		V_{CC1} = 12 V,	V_I = 12 V			1.0	μA
I_{IL}	Low-level input current		V_{CC1} = 12 V,	V_I = 0 V			−1.0	μA
I_{CC1}	Supply current				V_{CC1} = 4.5 V		4.0	mA
					V_{CC1} = 12 V		5.0	mA
I_{CC2}	Supply current		V_{CC1} = 5 V, V_{CC2} = 60 V		Outputs Hi		10.0	mA
					Ouputs Low		.5	mA

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 50pf See Figure 2		3.0	usec
t_{DLH}	Delay time, low-to-high-level output from strobe input			2.0	usec
t_{THL}	Transition time, high-to-low-level output			3.0	usec
t_{TLH}	Transition time, low-to-high-level output			1.0	usec

TYPICAL CHARACTERISTICS





PARAMETER MEASUREMENT INFORMATION

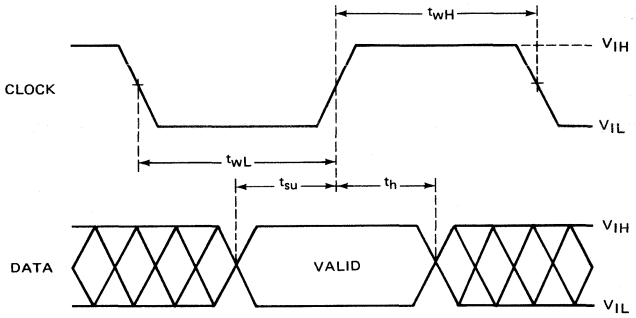


FIGURE 1 – INPUT TIMING VOLTAGE WAVEFORMS

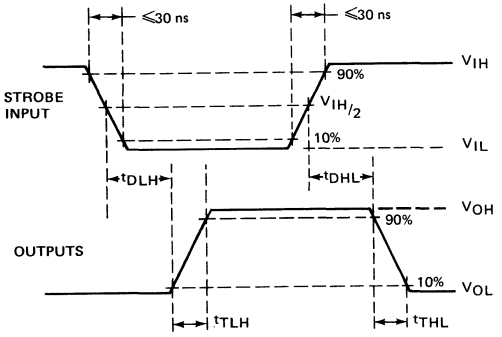


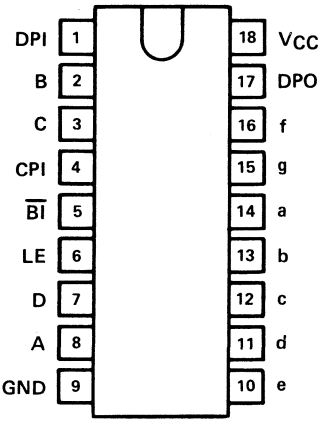
FIGURE 2 – SWITCHING-TIME VOLTAGE WAVEFORMS

TYPE SN75580
HIGH-VOLTAGE 7-SEGMENT LATCH/DECODER/CATHODE DRIVER

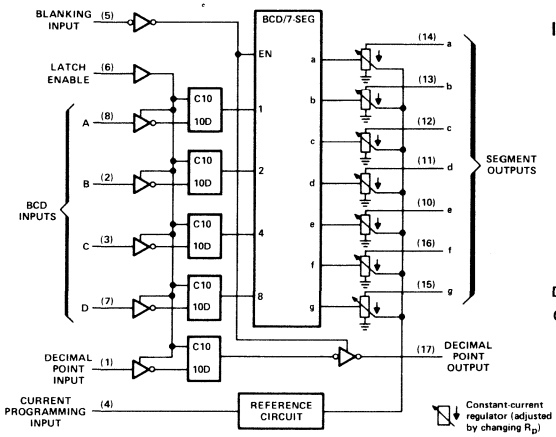
D2626, MAY 1981

- Output Current Adjustable From 0.1 mA to 1 mA
- DMOS Outputs for High Breakdown Voltage
  Segment Outputs . . . 100 V Min
  Decimal Point Output . . . 100 V Min
- Input Data Latches
- Blanking Input Provided
- Low Power Requirements
- Supply Voltage Variable over Wide Range . . . 5 V to 15 V
- Decimal Point Output Provided
- Suitable for Multiplex Operation

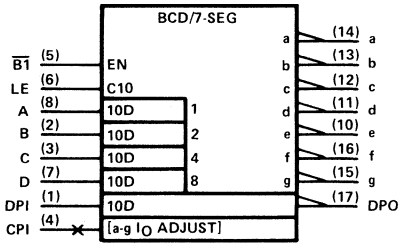
N
DUAL-IN-LINE PACKAGE (TOP VIEW)



functional block diagram



logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

description

The SN75580 is designed to decode four lines of BCD data and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. Latches are provided to store the BCD and decimal point data while the enable input is at a low-level voltage.

The design employs a read-only memory to provide output decoding for the BCD digits 0 to 9. For input data greater than BCD 9, the segment outputs are blanked. Each sink output is regulated to ensure a constant brightness of the display even with a fluctuating supply voltage. The on-state output current is essentially constant over the output voltage range of 4 volts to 100 volts. Each current sink is ratioed to the "b" segment output current as required for even illumination of all segments.

†Trademark of Burroughs Corporation.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

description (continued)

Output currents may be varied from 0.1 mA to 1 mA for driving various displays. The output current is adjusted by connecting an external programming resistor (R_p) from the current programming input to ground.

The blanking input provides unconditional blanking of all segment outputs including the decimal point output.

The enable input allows data to be stored internally while input data is changing. When enable is at a high-level voltage, the outputs will reflect conditions on the A, B, C, D, and DP inputs. A transition from a high-level voltage to a low-level voltage at enable will cause the input data set up prior to the transistion to be latched. In the latched state, the A, B, C, D, and DP inputs are in a high-impedance state to minimize input loading.

FUNCTION TABLE

SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	DP INPUT†	BCD INPUTS†				BI	SEGMENT OUTPUTS							DP OUTPUT	DISPLAY
		D	C	B	A		a	b	c	d	e	f	g		
0	X	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	X	
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	X	
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	X	
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	X	
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	X	
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	X	
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	X	
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	X	
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	X	
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	X	
10	X	H	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
11	X	H	L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
12	X	H	H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
13	X	H	H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
14	X	H	H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
15	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
DP	H	X	X	X	X	H	X	X	X	X	X	X	X	ON	
DP	L	X	X	X	X	H	X	X	X	X	X	X	X	OFF	

H = high level, L = low level, X = irrelevant

†Table is valid for the indicated BCD and decimal point inputs while the latch enable is high. See description.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Input voltage . . . . . V_{CC}
Peak transient off-state voltage, segment outputs (See Note 2) . . . . . 180 V
Continuous on-state segment output current . . . . . 4 mA
Peak transient on-state segment output current (See Note 3) . . . . . 50 mA
Continuous total dissipation . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In all applications, peak transient segment output voltage must be limited to 180 V. This is accomplished by limiting the anode voltage to 180 V maximum.
3. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10\ \mu s$, duty cycle $\leq 1\%$). This may be accomplished in d-c applications by connecting a 2.2 kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications (See Figure 4).

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	5	15	V
Segment output voltage	4	100	V
Decimal point output voltage	4	100	V
Segment-b output current	0.1	1	mA
Enable pulse width, t_w (see Figure 2)	500		ns
Data setup time before enable goes low (see Figure 2)	500		ns
Data hold time after enable goes low (see Figure 2)	500		ns
Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		V_{CC} = 10 V		7			V
V_{IL}	Low-level input voltage		V_{CC} = 10 V				3	V
V_{IK}	Input clamp voltage		V_{CC} = 15 V, I_I = −12 mA,	T_A = 25°C		−0.9	−1.5	V
$V_{O(on)}$	On-state output voltage	Decimal point	V_{CC} = 5 V, I_O = 25 mA				4	V
$V_{(BR)off}$	Off-state output breakdown voltage	a thru g	BI at 0 V, I_O = 3 μA		100			V
		Decimal point			100			
$I_{O(on)b}$	Segment-b on-state output current		V_{CC} = 10 V, $V_{O(b)}$ = 50 V, T_A = 25°C	R_p = 18080 Ω	0.17	0.20	0.23	mA
				R_p = 7232 Ω	0.425	0.50	0.575	
				R_p = 3616 Ω	0.85	1.00	1.15	
$\frac{I_{O(on)}}{I_{O(on)b}}$	Segment output currents normalized to b-segment current	Segments a, f, & g	V_{CC} = 10 V, All outputs at 50 V, T_A = 25°C		0.84	0.93	1.02	
		Segment c			1.12	1.25	1.38	
		Segment d			0.9	1.00	1.1	
		Segment e			0.99	1.10	1.21	
I_{IH}	High-level input current	All inputs except CPI	V_{CC} = 10 V, V_I = 10 V				1	μA
I_{IL}	Low-level input current	All inputs except CPI	V_{CC} = 10 V, V_{CC} = 0 V				1	μA
I_{CC}	Supply current		V_{CC} = 15 V, All inputs at 10 V, R_p open				4	mA
			V_{CC} = 15 V, All inputs at 0 V, R_p = 3.6 kΩ				6	

switching characteristics, V_{CC} = 10 V, T_A = 25°C, see figures 1 and 2

PARAMETER		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time of segment outputs from BCD inputs		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BCD inputs		0.5	10	
t_{off}	Turn-off time of segment outputs from DP input		0.5	10	µs
t_{on}	Turn-on time of segment outputs from DP input		0.5	10	
t_{off}	Turn-off time of segment outputs from BI		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BI		0.5	10	

PARAMETER MEASUREMENT INFORMATION

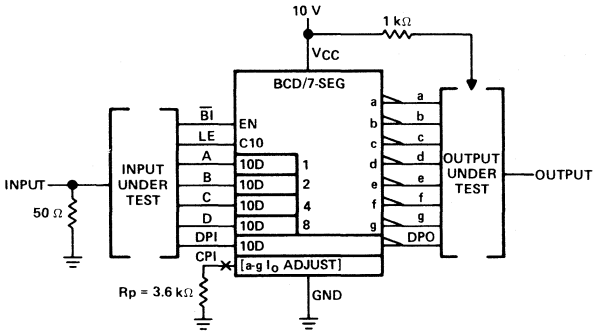


FIGURE 1–TEST CIRCUIT

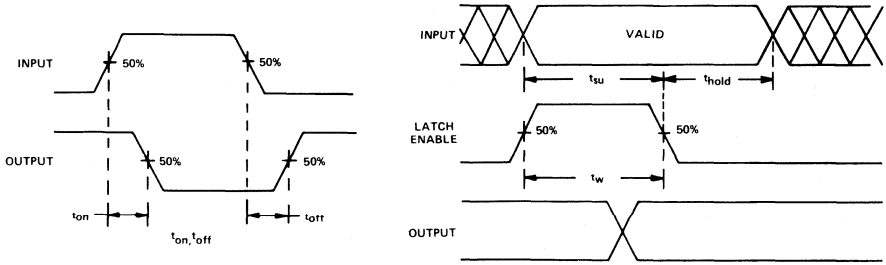


FIGURE 2–VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

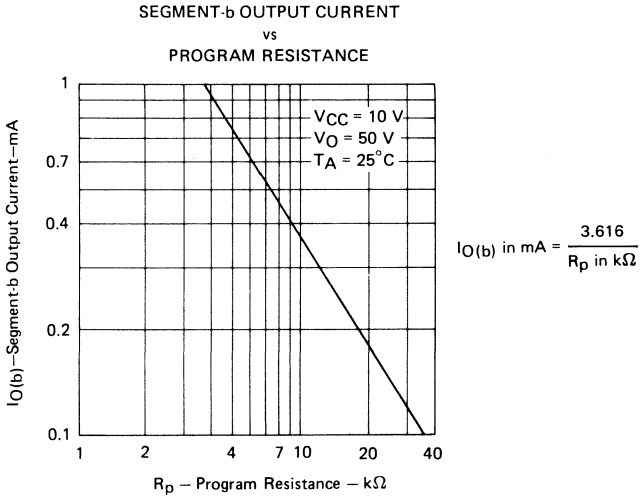


FIGURE 3

TYPICAL APPLICATION DATA

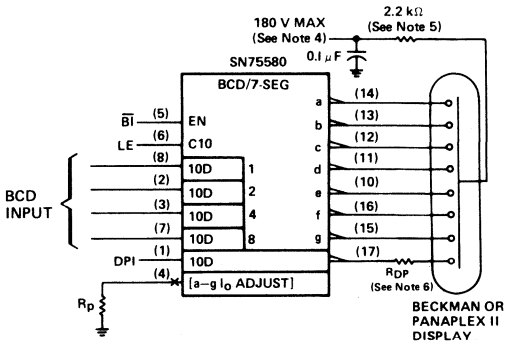


FIGURE 4—SINGLE-DIGIT 7-SEGMENT DISPLAY

NOTES: 4. This voltage must be adjusted for the type of display used to ensure that the on-state and off-state voltages do not exceed 100 V at the segment outputs of the SN75580.

5. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10$ μs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2-kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

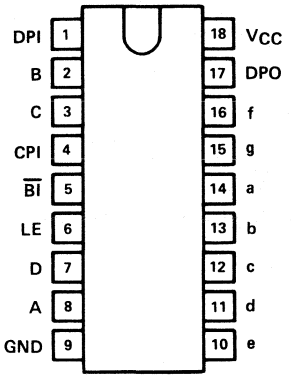
6. The value of R_{DP} is chosen for even illumination of the decimal point and the digit.

TYPE SN75584A HIGH-VOLTAGE 7-SEGMENT LATCH/DECODER/CATHODE DRIVER

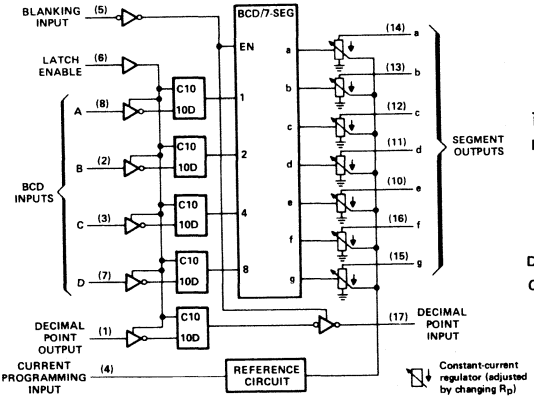
D2627, MAY 1981

- Output Current Adjustable From 0.1 mA to 4 mA
- DMOS Outputs for High Breakdown Voltage
  Segment Outputs . . . 100 V Min
  Decimal Point Output . . . 100 V Min
- Input Data Latches
- Blanking Input Provided
- P-N-P Inputs for Minimal Input Loading
- Low Power Requirements
- Thermal Protection Circuitry
- Supply Voltage Variable Over Wide Range . . . 4.75 V to 15 V
- Decimal Point Output Provided
- Suitable for Multiplex Operation

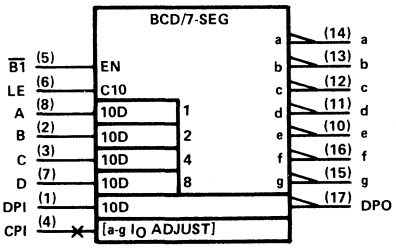
N
DUAL-IN-LINE PACKAGE (TOP VIEW)



functional block diagram



logic symbol †



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

description

The SN75584A is designed to decode four lines of BCD data and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. Latches are provided to store the BCD and decimal point data while the enable input is at a low-level voltage.

The design employs a read-only memory to provide output decoding for the BCD digits 0 to 9. For input data greater than BCD 9, the segment outputs are blanked. Each sink output is regulated to ensure a constant brightness of the display even with a fluctuating supply voltage. The on-state output current is essentially constant over the output voltage range of 4 volts to 100 volts. Each current sink is ratioed to the "b" segment output current as required for even illumination of all segments.

† Trademark of Burroughs Corporation.

description (continued)

Output currents may be varied from 0.1 mA to 4 mA for driving various displays. The output current is adjusted by connecting an external programming resistor (R_D) from the current programming input to ground.

The blanking input provides unconditional blanking of all segment outputs including the decimal point output.

The enable input allows data to be stored internally while input data is changing. When enable is at a high-level voltage, the outputs will reflect conditions on the A, B, C, D, and DP inputs. A transition from a high-level voltage to a low-level voltage at enable will cause the input data set up prior to the transition to be latched. In the latched state, the A, B, C, D, and DP inputs are in a high-impedance state to minimize input loading.

Thermal protection circuitry will blank the display, regardless of input conditions, whenever junction temperature exceeds approximately 150°C.

FUNCTION TABLE

SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	DP INPUT†	BCD INPUTS†				BI	SEGMENT OUTPUTS							DP OUTPUT	DISPLAY
		D	C	B	A		a	b	c	d	e	f	g		
0	X	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	X	
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	X	
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	X	
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	X	
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	X	
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	X	
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	X	
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	X	
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	X	
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	X	
10	X	H	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
11	X	H	L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
12	X	H	H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
13	X	H	H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
14	X	H	H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
15	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
DP	H	X	X	X	X	H	X	X	X	X	X	X	X	ON	
DP	L	X	X	X	X	H	X	X	X	X	X	X	X	OFF	

H = high level, L = low level, X = irrelevant

†Table is valid for the indicated BCD and decimal point inputs while enable is high. See description.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage	V_{CC}
Peak transient off-state voltage, segment outputs (See Note 2)	180 V
Continuous on-state segment output current	4 mA
Peak transient on-state segment output current (See Note 3)	50 mA
Continuous total dissipation	650 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. In all applications, peak transient segment output voltage must be limited to 180 V. This is accomplished by limiting the anode voltage to 180 V maximum.

3. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10$ µs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2 kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications (see Figure 4).

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.75	15	V
Segment output voltage	4	100	V
Decimal point output voltage	0	100	V
Segment-b output current	0.1	4	mA
Enable pulse width, t_w (see Figure 2)	500		ns
Data setup time before enable goes low (see Figure 2)	500		ns
Data hold time after enable goes low (see Figure 2)	500		ns
Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 15 V, I_I = −12 mA, T_A = 25°C			−0.9	−1.5	V
$V_{(BR)off}$	Off-state output breakdown voltage	a thru g	BI at 0 V, I_O = 3 μA		100			V
		Decimal point			100			
$I_{O(on)b}$	Segment-b on-state output current		V_{CC} = 10 V, $V_{O(b)}$ = 50 V, T_A = 25°C	R_p = 18080 Ω	0.18	0.20	0.22	mA
				R_p = 7232 Ω	0.45	0.50	0.55	
				R_p = 2411 Ω	1.35	1.5	1.65	
				R_p = 1808 Ω	1.8	2.0	2.2	
				R_p = 1205 Ω	2.7	3.0	3.3	
				R_p = 904 Ω	3.6	4.0	4.4	
			V_{CC} = 5 V to 15 V, $V_{O(b)}$ = 10 V to 100 V, T_A = 0°C to 70°C	R_p = 18080 Ω	0.16		0.24	
				R_p = 7232 Ω	0.4		0.6	
				R_p = 2411 Ω	1.2		1.8	
				R_p = 1808 Ω	1.6		2.4	
				R_p = 1205 Ω	2.4		3.6	
				R_p = 904 Ω	3.2		4.8	
$\frac{I_{O(on)}}{I_{O(on)b}}$	Segment output currents normalized to b-segment current	Segments a, f, & g	V_{CC} = 10 V, All outputs at 50 V, T_A = 25°C		0.84	0.93	1.02	
		Segment c			1.12	1.25	1.38	
		Segment d			0.9	1.00	1.1	
		Segment e			0.99	1.10	1.21	
		Segments a, f, & g	V_{CC} = 5 V to 15 V, All outputs at 10 V to 100 V, T_A = 0°C to 70°C		0.74		1.12	
		Segment c			1		1.5	
		Segment d			0.8		1.2	
		Segment e			0.88		1.32	
I_{IH}	High-level input current	All inputs	V_{CC} = 15 V, V_I = 15 V	Enable at 15 V			15	μA
		A, B, C, D, & DP		Enable at 0 V			1	
I_{IL}	Low-level input current	All inputs	V_{CC} = 15 V, V_I = 0.4 V	Enable at 15 V			−50	μA
		Enable		Enable at 0.4 V			−50	
		A, B, C, D, & DP		Enable at 0 V			−1	
I_{CC}	Supply current		V_{CC} = 15 V, All inputs at 15 V, R_p open				4	mA
			V_{CC} = 15 V, All inputs at 0 V, R_p = 2.2 kΩ				6	

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see figures 1 and 2

	PARAMETER	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time of segment outputs from BCD inputs		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BCD inputs		0.5	10	
t_{off}	Turn-off time of segment outputs from DP input		0.5	10	µs
t_{on}	Turn-on time of segment outputs from DP input		0.5	10	
t_{off}	Turn-off time of segment outputs from BI		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BI		0.5	10	

PARAMETER MEASUREMENT INFORMATION

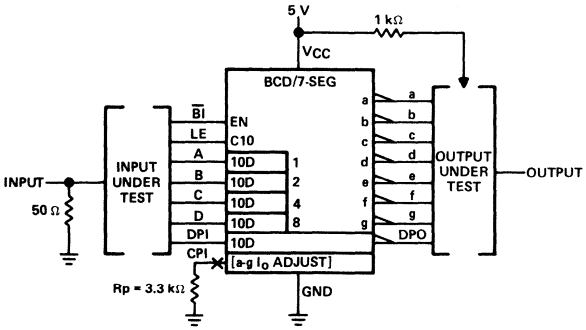


FIGURE 1 – TEST CIRCUIT

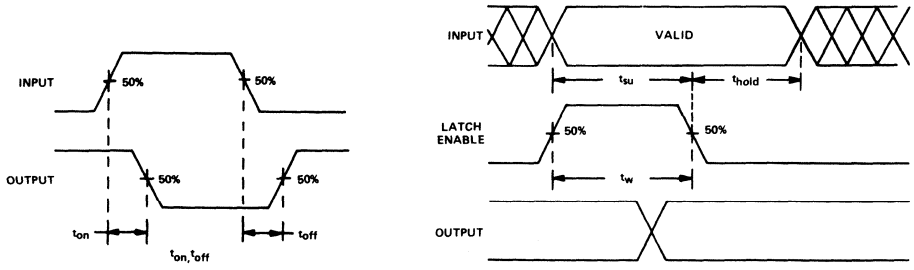
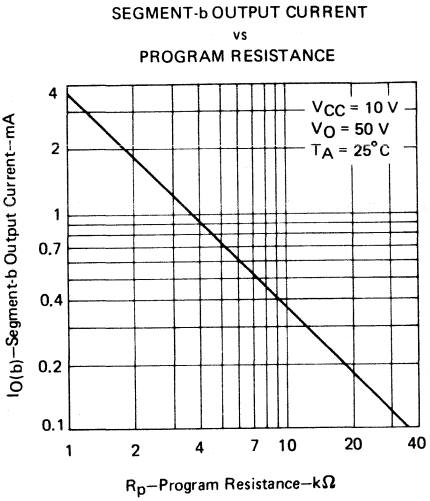


FIGURE 2–VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS



$$I_{O(b)} \text{ in mA} = \frac{3.616}{R_p \text{ in k}\Omega}$$

FIGURE 3

TYPICAL APPLICATION DATA

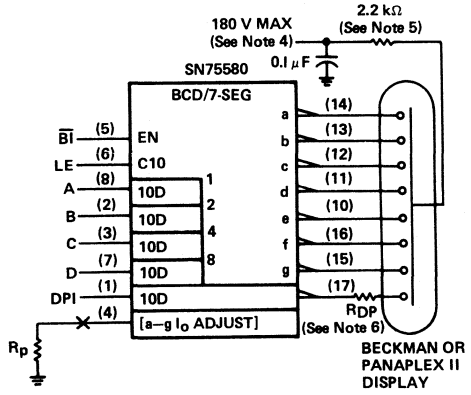


FIGURE 4—SINGLE-DIGIT 7-SEGMENT DISPLAY

NOTES: 4. This voltage must be adjusted for the type of display used to ensure that the on-state and off-state voltages do not exceed 100 V at the segment outputs of the SN75584A.

5. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10$ μs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2-kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

6. The value of R_{DP} is chosen as required for even illumination of the decimal point and the digit.

TL4810A BIDFET
10-Bit Serial-Input Latched Driver with Active Pull-Down

Features

- High-voltage outputs 60V
- CMOS compatible inputs
- Low power CMOS logic and latches
- Active pull-down outputs
- Wide supply voltage range
- Directly interchangeable with UCN4810A

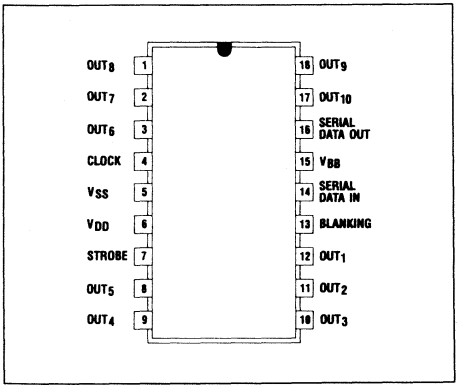
Description

The TL4810A is a monolithic BIDFET integrated circuit designed to drive a segmented, dot character, or full dot matrix vacuum fluorescent display (VFD).

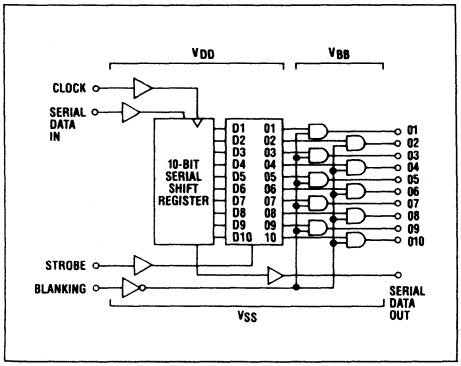
The primary feature of the TL4810A 10-bit VFD driver is its unique output structure. The TL4810A utilizes an active totem-pole output to improve the sink current capability without sacrificing the resulting power consumption as conventionally experienced in a passive pull-down structure. The totem-pole output decreases the inter-digit-blanking time required and the overall device power consumption.

Unlike most VFD drivers which are limited to an 85% duty cycle at 50°C the TL4810A will sustain a 25 mA per output load at 100% duty cycle over its entire operating temperature range of 70°C.

Designed to control 10 VFD inputs, the TL4810A contains a positive edge triggered 10-bit serial shift register with a serial data output for serial transmission and registration of the display information. A 10-bit D-type latch accepts parallel data from the serial shift register when the strobe input is high. The data stored in the latch circuitry when the strobe input is taken low remains un-altered regardless of subsequent changes in the data present in the serial shift register. The latched information is then transferred to the outputs through the gated output buffers when the blanking input is low. A logic high on the blanking input causes all outputs to go low. All outputs are capable of sourcing 40mA each at a supply voltage of 60V, providing the maximum allowable package power limitation is not exceeded. All device inputs are diode-clamped and compatible with standard MOS, CMOS and DMOS logic. The addition of a pull-up resistor to V_{DD} is required when driven by standard TTL logic.



N Dual-In-Line Package Pinout



TL4810 Functional Block Diagram

FUNCTIONAL TABLE

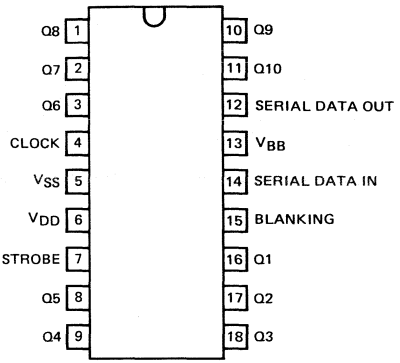
Function	Control Inputs*			Shift Register Contents R1 Thru R10	Latches Contents L1 Thru L10	Outputs	
	Clock	Strobe	Blanking			Serial	0-1 Thru 010
Load	⌐			Load and Shift	Determined by Strobe & R1/R10	R10	Determined By Blanking & L1/L10
	⌙			No Change			
Latch	X	High		As Determined Above	L1 = R1; L2 = R2; ETC	R10	Determined By Blanking & L1/L10
	X	Low			Stored Data		
Blanking			High	As Determined Above	As Determined Above	R10	All Low
			Low				10 = L1; 02 = L2; ETC

*All control inputs are independent of each other.

TYPE UCN-4810A VACUUM FLUORESCENT DISPLAY DRIVER

- Each Device Drives 10 Lines
- 60 V Output Voltage Swing Capability
- 40 mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs.

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

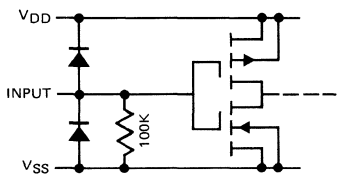
The UCN-4810A is a monolithic BIDFET+ integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display. (VFD)

Input data is stored in a 10-bit serial shift register on the positive transition of the clock. Parallel data is transferred to the output buffers through a 10-bit parallel D-type latch while the strobe input is high. Data present at the latches, input during a negative transition of the strobe, will be stored in the output regardless of subsequent data changes providing the strobe input is kept low. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors. The blanking input inhibits all output gates and assures they are off (low) when the blanking input is high.

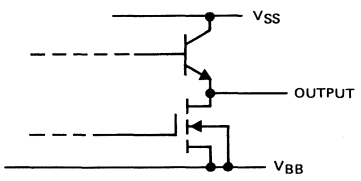
All inputs are CMOS and TTL compatible but require the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

Serial data output from the shift register may be used to cascade additional devices for large display arrays.

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



+BIDFET — Bipolar, Double Diffused, N-Channel and P-Channel MOS transistors on same chip — process patent pending.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TYPE UCN-4810A
VACUUM FLUORESCENT DISPLAY DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)

Supply voltage, V_{DD} (see note 1) . . . . . 4.5 V to 18 V
Supply voltage, V_{BB} . . . . . 5.0 V to 60 V
Input voltage . . . . . −.3 V to V_{DD}+ .3 V
Continuous output current, I_{out} . . . . . −40 mA
Continuous total dissipation at (or below) 70°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1.6 mm) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

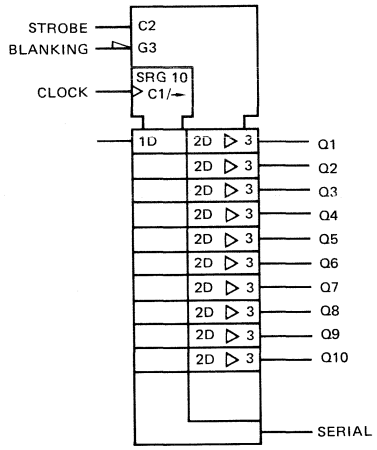
	MIN	NOM	MAX	UNITS
Supply voltage, V_{DD}	5		15	V
Supply voltage, V_{BB}	0		60	V
Continuous output current, I_{out}			−25	mA

electrical characteristics at T_a = 25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V (unless otherwise noted)

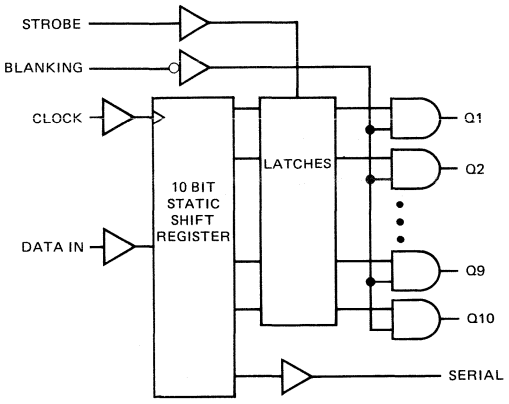
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Output OFF voltage	V_{out}		–	1.0	V
Output ON voltage		I_{out} = −25 mA	57.5		V
Output pull-down current	I_{out}	V_{out} = V_{BB}	−400	−850	μA
Output leakage current		Ta = 70°C	–	15	μA
Input voltage	$V_{in(1)}$	V_{DD} = 5 V	3.5	5.3	V
		V_{DD} = 15 V	13.5	15.5	V
	$V_{in(0)}$		−0.3	0.8	V
Input current	$I_{in(1)}$	V_{DD} = 5 V	–	100	μA
		V_{DD} = 15 V	–	300	μA
Input impedance	Z_{in}	V_{DD} = 5 V	50	–	K
Output resistance	R_{out}	V_{DD} = 5 V	–	20	K
		V_{DD} = 5 V	–	6	K
Supply current	I_{BB}	all outputs on	–	13	mA
		all outputs off	–	1.3	mA
	I_{DD}	V_{DD} = 5 V, Note 2	–	100	μA
		V_{DD} = 15 V, Note 2	–	200	μA
		V_{DD} = 5 V, Note 3	–	1.0	mA
		V_{DD} = 15 V, Note 3	–	3.0	mA

Note 2 all outputs off, all inputs = 0 V Note 3 one output on, all inputs = 0 V

logic symbol‡

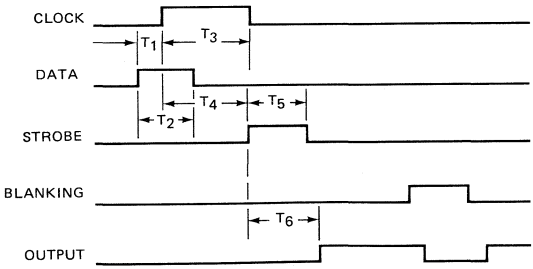


functional block diagram



‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

TIMING CONDITIONS	V_{dd} = 5 V	V_{dd} = 15 V
T1 – Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
T2 – Minimum Data Pulse Width	500 ns	300 ns
T3 – Minimum Clock Pulse Width	1.0 us	250 ns
T4 – Minimum Time Between Clock Activation and Strobe	1.0 us	400 ns
T5 – Minimum Strobe Pulse Width	500 ns	300 ns
T6 – Typical Time Between Strobe Activation and Output Transition	1.0 us	1.0 us



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